Transport properties and low-frequency noise in low-dimensional structures

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Transport properties and low-frequency noise in low-dimensional structures

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There's Plenty of Room at the Bottom.

Richard Feynman

... and still

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Abstract

Recently, a keyword of complementary metal-oxide-semiconductor (CMOS) technology for the higher performance, lower power consumption, larger device integration, and cost reduction is “down-scaling” leading low-dimensional structures. For the various applications with low-dimensional structures, a great deal of research is being carried out to understand their electrical and physical properties. Particularly, low-frequency noise in conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) has been well known to relate the signal fluctuations by the carrier trapping and de-trapping at the oxide-semiconductor interface. However, for low-dimensional structures, the noise properties are not sufficiently investigated. In this dissertation, the carrier transport and low-frequency noise properties in low-dimensional FET structures, which are fabricated by top-down or bottom-up approach, are investigated depending on high-k materials, conduction mechanism, strain engineering, metal-semiconductor junctions, and scatterings.

At the beginning of the dissertation, in chapter 1, the current issues of the device scaling in CMOS technology are reviewed and the low-dimensional structures are introduced with two representative approaches (i.e. top-down and bottom-up approaches). The electrical transport and low-frequency noise properties in low-dimensional structures are also discussed for the applications. In chapter 2, important device parameters of conventional FET structures such as threshold voltage, mobility, series resistance, subthreshold swing, and capacitance are defined and their practical extraction methods are presented. In chapter 3, the fundamental noise and representative low-frequency noise models for FET structures are introduced. One is the mobility fluctuation model (HMF) due to the carrier scattering and the other is the carrier number fluctuation model (CNF) considering the correlated mobility fluctuations (CMF) mainly affected by the trapping/release of charge carriers. In addition, the system configuration and helpful advices for the noise measurement are also discussed.

Experimental results of the transport properties and low-frequency noise in multi-gate FETs (FinFET and junctionless FET), Si and SiGe core-shell nanowire gate-all-around FETs, multi-walled carbon nanotube devices, and graphene FET are presented from chapter 4 to chapter 6. First, the multi-gate FET is a noticeable device recently introduced to reduce the short-channel effects. In this study, two kinds of multi-gate FETs are investigated: a FinFET is well-known as a multi-gate FET having a surface conduction by channel inversion whereas

a junctionless FET is operated by the highly doped channel i.e. bulk conduction. The bulk conduction is expected that the noise comes from the mobility fluctuations. But, interestingly, the low-frequency noise in junctionless FET is also explained by the carrier number fluctuation model same as the FinFET. The noise origin is estimated to have different mechanisms. For the FinFET, it is due to the carrier trapping and de-trapping at the oxide-semiconductor interface while the noise in junctionless FET is affected by carrier trapping at the boundary between the channel and depletion region (i.e. Schottky-Read-Hall generation-recombination).

For the nanowire and nanotube structures, the impact of channel strain and metal contact on the low-frequency noise is observed. Three-dimensional (3-D) stacked Si and SiGe core-shell nanowire gate-all-around FETs were compared with compressively strained and un-strained devices. Even though the c-strained devices have inhomogeneous trap distribution in long channel devices, the trap densities of both devices are similar. However, the c-strained ones effectively reduce the influence of correlated mobility fluctuations by the carrier confinement far from the oxide/Si cap interface. Next, the influence of metal-semiconductor junction is studied with different metal contacts based on the noise analysis. The existence of Schottky barrier due to the work function difference shows different relationship for the low-frequency noise and the device resistance. It indicates that contact metal for nanowire can strongly affect the noise properties of low-dimensional structures. Using low-frequency noise measurement, the quality of metal contact on the GaN nanowire is analyzed and it shows that the noise measurement can be a useful tool to assessment the device quality and reliability.

As a perfect 2-D structure, Graphene is an interesting material having surprising high carrier mobility, massless electrons, and a zero band gap. However, graphene FETs fabricated on the substrate exhibit strongly degraded mobility due to the significant impact of carrier scattering. Considering the influence of substrate for the graphene channel, low-frequency noise in graphene FETs is investigated. The noise in single layer graphene FETs exhibits M-shaped behavior as a function of the gate voltage and its behavior is similar to the transconductance variation partially limited by the scattering from the substrate.

In conclusion, it is confirmed that low-frequency noise in FET structures are severely affected by the quality of gate dielectric irrespective of conduction mechanism. Nevertheless, it shows that the noise can be controlled and reduced by applying channel strain or using appropriate metal contact electrode. In the case of graphene transistors, it exhibits quite different noise behavior that is estimated by the carrier scattering on the substrate. Such

results will be helpful for the study of the carrier dynamics fundamental in low-dimensional structures and intense related research. Especially, the noise limits the performance of low-noise devices or sensor applications as decreasing the device size so that the noise should be considered for the future study of low-dimensional structures and their applications.

Keywords: low-frequency noise, 1/f noise, fluctuation, field-effect transistor, trap density, scattering, low-dimensional structure, top-down, bottom-up, FinFET, junctionless FET, SiGe nanowire, multi-walled carbon nanotube, graphene

Theoretical Background

Chapter 1 Introduction to low-dimensional structures

Chapter 2 Electrical properties for FET structures

Chapter 3 Low-frequency noise characterization

Chapter 1 Introduction to low-dimensional structures

1.1 Scaling overview

The semiconductor technology has achieved a remarkable growth over the past half-century since the development of “transistor” by W. Shockley, J. Bardeen, and W. Brattain in 1947 [1] and the invention of integrated circuit (IC) by J. Kilby (1958) accelerated the growth of semiconductor industry and technology based on silicon. The number of transistors integrated on the same area dramatically increased from several tens to billions and the high-integrated semiconductor devices lead to the miniaturization of electronic products such as TV/VCR, computer, mobile phone, and other e-portable products. Finally, most products use semiconductor devices. For the high-performance of electronic applications, transistors were scaled down continuously and the efforts opened the era of nano devices. Nano devices have many advantages over than microscale counterpart for the performance, the power consumption, the integration and the application. Especially, the quantum transport by the channel confinement and the ballistic transport in which electrons cannot be scattered owing to low-dimensional structures are also noteworthy [2].

However, the device scaling also brought new challenges to overcome in terms of materials, device structures, fabrication technologies, performances, noise, reliability, and so on. For example, the conventional planar complementary metal-oxide-semiconductor (CMOS) technology appeared additional problems usually called “short-channel effects” as decreasing the channel size. The short-channel effects are secondary effects which refer to typically the source/drain charge sharing, the drain-induced barrier lowering, and the subsurface punchthrough [3]. The impact of short-channel effects is to reduce the threshold voltage of the devices so that it interferes with the normal operation of the devices. The limitation of optical lithography technology in wavelength and the alternatives of channel and gate oxide materials must be considered as well.

Figure 1.1 shows the graphical trends for the device scaling of International Technology Roadmap for Semiconductors (ITRS) 2010 reports [4]. The gate length of transistors should be sub 10 nm scales within 10 years. The gate-stack materials will maintain the use of high-k

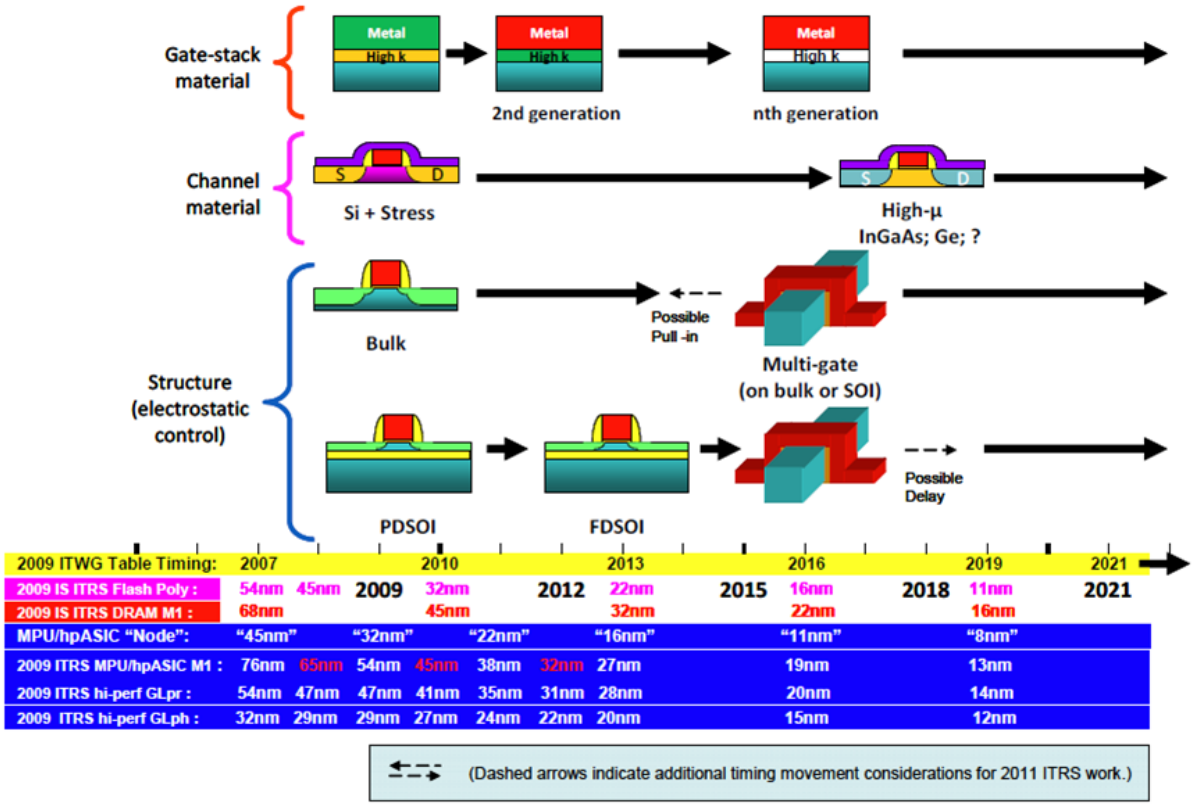


Figure 1.1 ITRS Overall Roadmap Technology Characteristics (ORTC) graphical trends including overlay of 2009 industry logic "nodes" and ITRS trends for comparison [4].

materials instead of silicon oxide for better gate control and lower gate leakage current. For the high-speed devices, the channel has also been studied applying channel strain on silicon or supplanting the materials with Ge or III-V compound semiconductors that have higher mobility than silicon. To reduce the short-channel effects and obtain improved electrostatic control of devices, multi-gate structures have been proposed for the scaling away from the conventional planar technology [5]. Even if early multi-gate structures have been fabricated on the silicon on insulator (SOI) substrate, many studies are also in progress on bulk substrate [6], [7]. Besides studies based on silicon, there are many attempts and studies with nanowires and nanotubes for the next-generation semiconductor device.

As decreasing the channel structure close to quasi one-dimensional (1-D) structures, their physical and electrical properties are represented based on quantum mechanics. It is also complicated due to the structural features such as coupling effect, electrostatic control and surface effect. Therefore, for the successful device scaling, low-dimensional structures should be understood and studied.

1.2 1-D and 2-D structures

Low-dimensional structures came to the notice of the scientific community in the early 1970s when L. Esaki and R. Tsu suggested the fabrication of superlattices by epitaxial growth to realize negative-differential-conductivity devices appearing Bloch oscillations [8]. In the case of electronic transport, low-dimensional structure refers to a system in which the charge carriers (e.g. electron) are constrained by potential barriers so that their motion will be suppressed [9]. It can be classified into two-, one- or zero-dimensional structures depending on whether the potential barriers confine the electrons in one-, two-, or three- dimensions, respectively. Figure 1.2 represents illustrations of low-dimensional structures. It is noted that there is no absolute value of length to define the dimensionality and the length is just related to determine the physical properties of dimensionality in semiconductors such as Debye length, scattering length and so on [9].

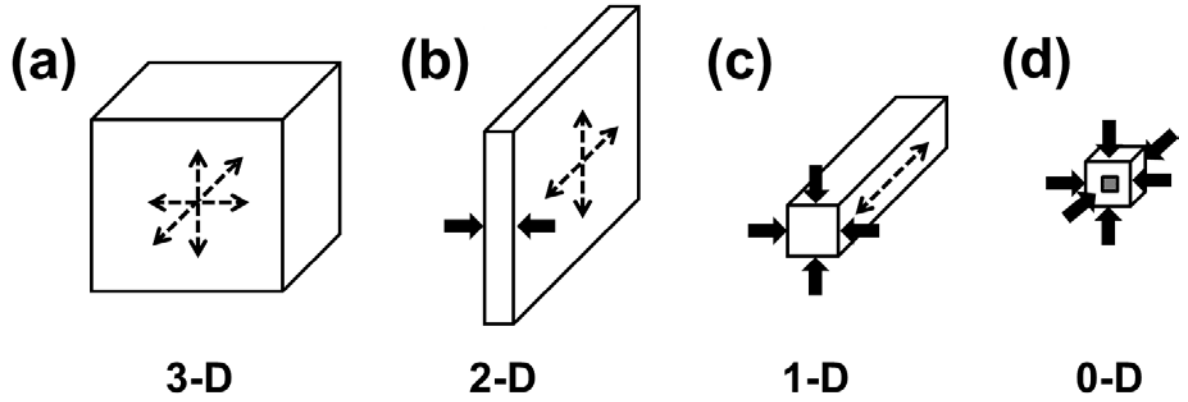


Figure 1.2 Illustrations of low-dimensional structures: (a) bulk semiconductors (b) thin films, quantum wells (c) linear chain structures, quantum wires (d) quantum dots. A dotted line displays the freedom degree of carrier transport.

In CMOS technology, the conventional planar devices gradually changes to low-dimensional structured devices with the downscaling of the gate length. Contrary to bulk structured devices, 1-D and 2-D structures have novel physical and electrical properties. Electrons in materials show different electrical behavior such as the insulator, the semiconductor, and the metal depending on the materials size because they have different energy spacing of the eigenstates. For this reason, low-dimensional structures have been concerned by many scientists for a long time. In 1991, the discovery of carbon nanotubes as a 1-D nanostructure by S. Iigima [10] inaugurated an era of nanotechnology and accelerated it. In addition, metal oxide 1-D nanostructures such as ZnO, SnO_2, Cu_2O, Fe_2O_3, and CeO_2 have

investigated for the size and dimensionality dependence of nanostructure properties for their applications [11]. In 2004, the electrical property of monocrystalline graphitic films, so called "graphene" as a 2-D nanostructure reported by K. S. Novoselov and A. K. Geim [12]. Graphene is a flat monolayer of carbon atoms tightly packed into a 2-D honeycomb lattice, and it is a basic building block for graphitic materials of all other dimensionalities (Figure 1.3) [13]. More than 70 years ago, L. D. Landau and R. E. Peierls discussed that strictly 2-D crystals were thermodynamically unstable and could not exist owing to a divergent contribution of thermal fluctuations in low-dimensional crystal lattices [14-16]. Due to the difficulty of being 2-D crystals in ambient conditions, the study of 2-D structures was limited as a two-dimensional electron gas (2DEG) which is a gas of electrons free to move in two-dimensions [17]. However, various 2-D nanostructures can also be studied together with the successful exfoliation of graphene [18]. Recently, many studies of low-dimensional structures such as nanowires, nanotubes, and graphene have been carried out in various view points for the synthesis, device fabrication, characterization, and their applications.

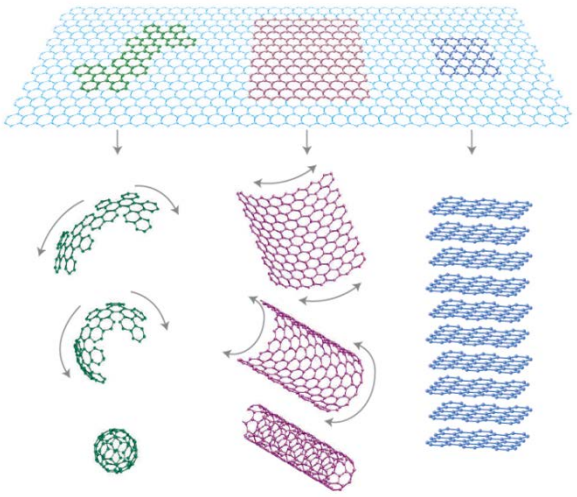


Figure 1.3 Mother of all graphitic forms [13].

1.3 Top-down vs. Bottom-up approaches

To fabricate 1-D and 2-D nanostructures such as nanowires, nanotubes and graphene (or other 2-D metal films), there are two representative approaches: one is the 'top-down' approach and the other is the 'bottom-up' approach. The top-down approach stands for the geometrical shaping and carving of solid materials from outside to inside whereas the bottom-up approach represents the structure growth by the increase of anisotropy from the atomic scale. Figure 1.4 shows the SEM images for SiGe [19] and ZnO nanowires [20] by top-down and bottom-up approach.

In detail, the top-down approach is based on the conventional semiconductor manufacturing processes consisting of film formation, impurity doping, lithography and

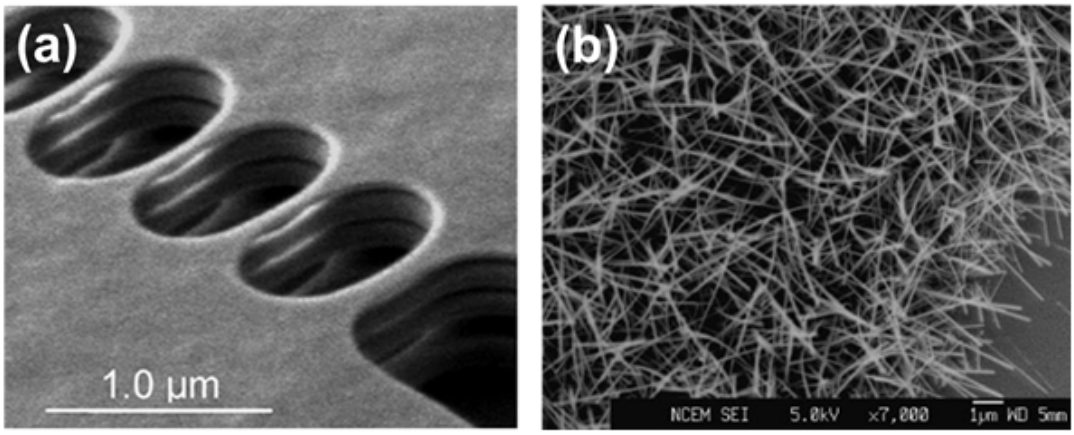


Figure 1.4 Scanning electron microscopy (SEM) images of (a) top-down processed stacked SiGe nanowires [19] **and (b) ZnO nanowires grown on Si (100) substrate [20].**

etching with various mask sets on the silicon substrate and most of semiconductor devices have been fabricated by this approach. For the realization of 1-D and 2-D nanostructures, the advanced lithography techniques that can be possible to make a pattern for narrow feature size (i.e. nanometer scale) and improved etching methods for the various dimensional structures are also required in the top-down approach. For this, electron-beam (e-beam) lithography, X-ray lithography, or immersion lithography systems were developed for drawing the nm-scale pattern [21-23]. In recent years, improved lithography systems and etching techniques have been applied for the next-generation metal-oxide-semiconductor field-effect transistors (MOSFETs) such as Double-Gate (DG) MOSFETs, FinFETs, and Gate-All-Around (GAA) FETs equivalent to 1-D or 2-D nanostructures. The top-down approach for nanostructures still guarantees the mass production and the reproducibility without many changes of existing fabrication processes. However, it needs high processing cost and well-defined large space for the equipment.

In the different point of view, the bottom-up approach generally indicates the chemically anisotropical growth of nanostructures from the atomic size. For anisotropical growth of crystal, the most well-known method in the bottom-up approach is the Vapor-Liquid-Solid (VLS) [24]. The VLS method is used for the crystal growth with direct adsorption of a gas phase on the substrate with slow chemical process

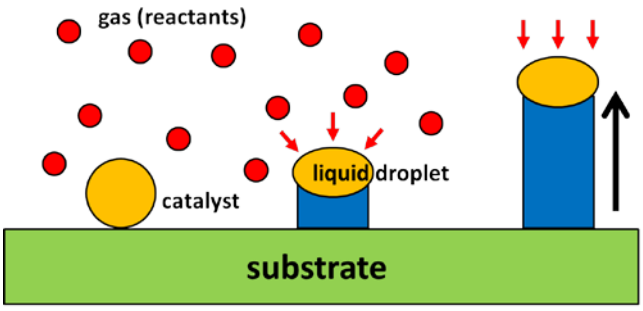


Figure 1.5 Schematic illustration of bottom-up grown nanowire by Vapor-Liquid-Solid (VLS) process.

as shown in Figure 1.5. The various size and length of nanowires can be grown by VLS method having a single crystal structure depending on the growth conditions.

After growth of nanowires on the substrate, the nanowire separation, purification, and post-growth techniques are required to select the proper size of nanowires and transfer to the substrate for the device fabrication through the dispersion process. And then metal electrodes are deposited to investigate their electrical properties. One of the difficulties for the device fabrication with an individual nanowire is the nanowire manipulation and accurate patterning for metallization because of their small size. There are some typical methods such as photo lithography, e-beam lithography or self-assembly technique for selective patterning [25]. E-beam lithography is typically used for metallization even if there are some difficulties to make selective patterns on the nanowire precisely. But a simple selective e-beam patterning technique with an optical microscope or a Scanning Electron Microscope (SEM) images enables it easy single nanowire pattern [26]. The bottom-up approach cannot guarantee the mass-production and the reproducibility due to the difficulties above-mentioned. But this approach is favorable to study intrinsic properties of nanostructures that are more close to 1-D or 2-D structures than ones made by a top-down technique.

1.4 Electrical issues in low-dimensional structures

Low-dimensional structures have some interesting electrical phenomena such as an electron tunneling and a quantization of electronic states. The electron tunneling is a quantum mechanical phenomenon where a particle (e.g. an electron) can tunnel through a potential barrier at the quantum scale. It is used for the tunneling diode applications. On the other hand, the electron and its energy state are limited and quantized by the dimensionality. Electronic behaviors in a solid are determined by the density of state at the Fermi energy. The energy

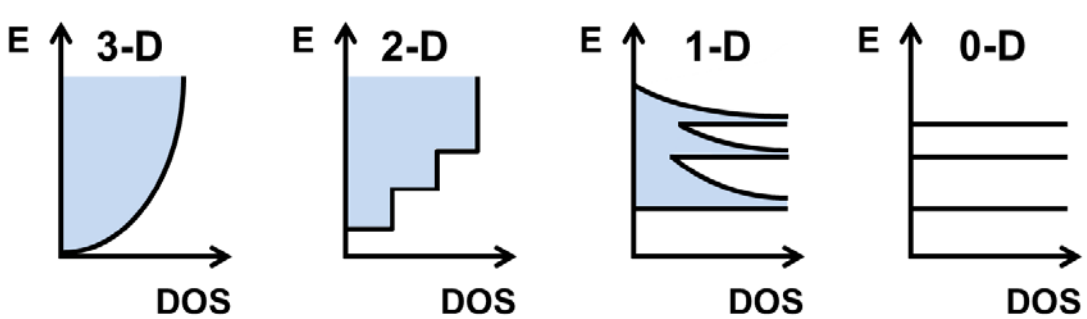


Figure 1.6 Density of states (DOS) in low-dimensional (2-D, 1-D, 0-D) semiconductor structures.

dispersion in a bulk and low-dimensional structures are illustrated in Figure 1.6 [27]. Many electrical and physical properties in low-dimensional structures are expected to have better performances for nano electronics. To achieve low-dimensional structures by top-down or bottom-up approaches, there are some practical issues which should be considered.

For low-dimensional structure devices with conventional CMOS technology, an important issue is short-channel effects. The short-channel effects induced a leakage current in the off-state thereby increase the power consumption for the idle state. To reduce the short-channel effects and obtain the better gate control, nanowire channels with a gate-all-around structure are seen as an ideal transistor channel [28]. According to the device scaling, the channel is approaching 1-D structures which have large surface/volume ratio. The large surface/volume ratio is advantageous for sensor applications but it can also affects the electronic transport due to surface effects. The surface roughness control is one of the difficulties for nanostructures with top-down process and it can be a source of trapping center of charge carriers or mobility degradation by scatterings. The electrical noise, especially $1/f$ noise, is another issue for device scaling. As decreasing the device size, the $1/f$ noise is expected to increase because the relative noise spectral density is inversely proportional to the effective size of devices [29], [30]. The $1/f$ noise in the drain current or gate voltage of a MOSFET has been an important role for analog circuits and RF applications which are related to the signal to noise ratio (SNR) and the phase noise of oscillators, respectively [31]. Many studies for nanotubes and nanowires have been reported to exhibit significant current fluctuations in the low-frequency regime [32-39].

On the other hand, a Schottky barrier between the metal and semiconductor is a notable issue when we make a device with bottom-up growth nanowires. In general, metal electrodes are commonly used in a nanowire device unlike conventional MOSFETs having source/drain contacts with degenerated doped silicon. It is due to the difference of preferred fabrication process with nanowires [40]. For this reason, the existence of Schottky barrier in nanowire devices is inevitable. These contacts can be improved after thermal annealing process but it still limits the device performance and disturbs the intrinsic properties of the nanostructures.

1.5 Outline of the thesis

In this thesis, the electrical properties of low-dimensional FET structures are investigated in the view point of top-down and bottom up approaches. Especially, low-frequency noise is

intensively characterized along with the electrical analysis of devices. Using the low-frequency noise characterization, the carrier dynamics that cannot be observed with normal electrical characterization is understood. Moreover, the low-frequency noise characterization is examined as a tool to determine the device quality. According to these objectives, the manuscript is structured as follows;

We have introduced the recent trends of CMOS technology and the device scaling issues are browsed roughly. To overcome the current limits of device scaling, the low-dimensional FET structures are discussed for their fabrication and electrical issues. Chapter 2 introduces some important parameters such as the threshold voltage, the mobility, the series resistance, the subthreshold swing, and the capacitance to understand the transport properties of nanowire and nanotube devices. The low-frequency noise is introduced in chapter 3 together with the history, the mathematical concept, the fundamentals, and the noise measurement system configuration. The well-known 1/*f* noise models for FET structures which are the carrier number fluctuation and the mobility fluctuation model are presented.

From chapter 4 to chapter 6, experimental results of static and 1/*f* noise properties are discussed for 1-D and 2-D nanostructures; Multi-gate MOSFETs (Chapter 4), Si and SiGe nanowire FETs and carbon nanotube devices (Chapter 5), and graphene FETs (Chapter 6). In chapter 4, FinFETs and junctionless FETs are examined with different channel length and width. The 1/*f* noise origin is compared between the FinFET and the junctionless FET which have the surface conduction and the bulk conduction, respectively. In chapter 5, the 1/*f* and RTS noise properties in Si and SiGe gate-all-around (GAA) FETs depending on the channel strain effect and the influence of junctions in GaN nanowire and carbon nanotubes are described. In chapter 6, the basic physics and 1/*f* noise analysis of graphene FETs are arranged separately because the graphene exhibits significantly different physical behaviors compared with other semiconductors. Finally, the summary of all experiment results is concluded in chapter 7.

Chapter 2 Electrical properties for FET structures

2.1 Introduction

The electrical measurement is the most-common method to understand the physical and electrical properties in semiconductors and their applications. Fundamentally, it has been understood with Ohm's law, giving the relationship between the voltage and the current in an electrical conductor. In detail, the electrical behavior depends on the conductivity (or resistivity) which is an intrinsic property determined by electrons in a solid. So, the electrical measurement will be helpful to understand the carrier dynamics in solid-states and to provide useful information for the applications. In general, it is classified as two different standpoints: one is a DC (direct current) measurement directly correlated to the resistance. It is mainly obtained with the current-voltage (*I*-*V*) measurement. The other is an AC (alternating current) measurement for the electrical impedance which can be understood as a kind of the resistance for the AC signal. The capacitance-voltage (*C*-*V*) measurement is normally used. Based on Ohms' law, the *I*-*V* measurement reveals a driving current, a conductance, a carrier mobility and so forth which are directly related to the device performance. On the other hand, the *C*-*V* measurement refers to one of the impedance spectroscopy and it can give more accurate information of charge carrier concentrations at the interface as well as in the bulk semiconductor.

In conventional MOSFETs, the electrical characterization has been used to extract device parameters to confirm the device performance and to apply to the logic devices. Such parameters as threshold voltage, mobility, carrier concentration, interface charge, series resistance can be extracted. In an era of nanotechnology, the electrical characterization is still important and relevant even though the device dimension is decreased approaching an atomic scale and the electronic transport is approaching to the quantum mechanics. Moreover, the improved model for nano-scale devices is needed considering additional effects as reducing the device size. In this chapter, several important parameters for the characterization of MOSFET structure devices such as threshold voltage, mobility, series resistance, capacitance, subthreshold swing and their detailed method will be summarized.

2.2 Threshold voltage

For understanding the MOSFET operation, threshold voltage (V_{TH}) is the most important and fundamental device parameter and the precisely controlling of threshold voltage is a major issue in most CMOS integrated-circuit applications [3]. The definition of threshold voltage, firstly suggested in 1953 [41], is commonly understood as the gate voltage when the energy band bending at the Si-SiO_2 interface is equal to twice the potential in bulk semiconductors [42] as shown in Figure 2.1. The surface potential ϕ_S on the *p*-type substrate (i.e. an n-channel MOSFET) for the threshold voltage is given by

$$\phi_S = 2\phi_F = \frac{2kT}{q}\ln\left(\frac{p}{n_i}\right) \approx \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{2.1}$$

where ϕ_F is the bulk potential, n_i the intrinsic carrier density, p the hole density, and N_A the acceptor doping density. It corresponds to the gate voltage for which the channel is opened to the current flow.

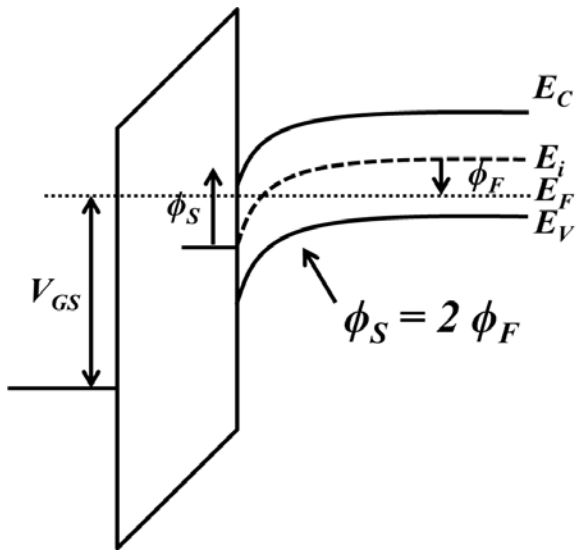


Figure 2.1 Band diagram for threshold voltage in enhancement-mode *n*-channel MOSFET.

In detail, the conventional enhancement-mode n-channel MOSFET is comprised of a *p*-type silicon substrate. As increasing the gate voltage V_{GS}, the electrons start to be drawn at oxide-semiconductor interface by the electric field against the holes that are away from the interface. As a result, the *n*-type channel in *p*-type silicon substrate is formed if the electric field is sufficient. The channel region is called an inversion layer. Before the formation of sufficient inversion layer, the current cannot flow (i.e. turn-off) even though the current that is called the subthreshold current still exists by diffusion. Therefore, the threshold voltage determines the device operation which means the formation of the channel layer for the conduction. An expression for the threshold voltage in the n-channel MOSFET on uniformly doped substrate without any short channel or other effects can be derived as

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\varepsilon_S\varepsilon_0 N_A(2\phi_F - V_{BS})}}{C_{OX}} \tag{2.2}$$

where V_{FB} is the flat-band voltage, ε_S the relative permittivity of silicon, ε_0 the vacuum permittivity, C_{OX} the oxide capacitance, and V_{BS} the substrate-source voltage. For an ideal MOS system (i.e. no charges at the oxide and Si-SiO_2 interface), the flat-band voltage can be determined as

$$V_{FB} = \Phi_M - \Phi_S = \Phi_{MS} \tag{2.3}$$

where Φ_M is the metal work function and Φ_S the semiconductor work function. However, for a real MOS system, the flat-band voltage is further affected by several charges at the oxide and interface. Therefore, Equation 2.3 becomes

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{OX}} - \frac{Q_{it}(\phi_S)}{C_{OX}} - \frac{1}{C_{OX}}\int_0^{t_{OX}} \frac{x}{t_{OX}}\rho_m(x)dx - \frac{1}{C_{OX}}\int_0^{t_{OX}} \frac{x}{t_{OX}}\rho_{ot}(x)dx \tag{2.4}$$

where Q_f is the fixed charge at the Si-SiO_2 interface, Q_{it} the interface trapped charge depends on the surface potential ϕ_S, $\rho_m(x)$ and $p_{ot}(x)$ are the mobile and oxide trapped charges distributed along the oxide. These additional charges from the oxide and the interface are important for the threshold voltage. In practice, the threshold voltage can be derived from the MOSFET characteristics through I_D-V_{GS} measurement. There are numerous methods for the threshold voltage extraction [42-46] and some well-known extraction methods are introduced in here. However, it is noted that each method is not always good for all kinds of transistors, particularly nano-scale transistors. Hence, to obtain more accurate value of threshold voltage, the threshold voltages from several methods should be compared considering the transport mechanism depending on the device structures and materials.

2.2.1 Linear extrapolation method

The most classical method is a linear extrapolation method, which is an old style but well-known, using a linear fit at the maximum transconductance, $g_{m,\,max}$ from I_D-V_{GS} characteristics at the linear region. At strong inversion, the drain current can be expressed as

$$I_D = \frac{W}{L}\mu_{eff}C_{OX}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{2.5}$$

where W is the channel width, L the channel length, and μ_{eff} the effective mobility. If V_{DS} is small enough, Equation 2.5 can be simplified to

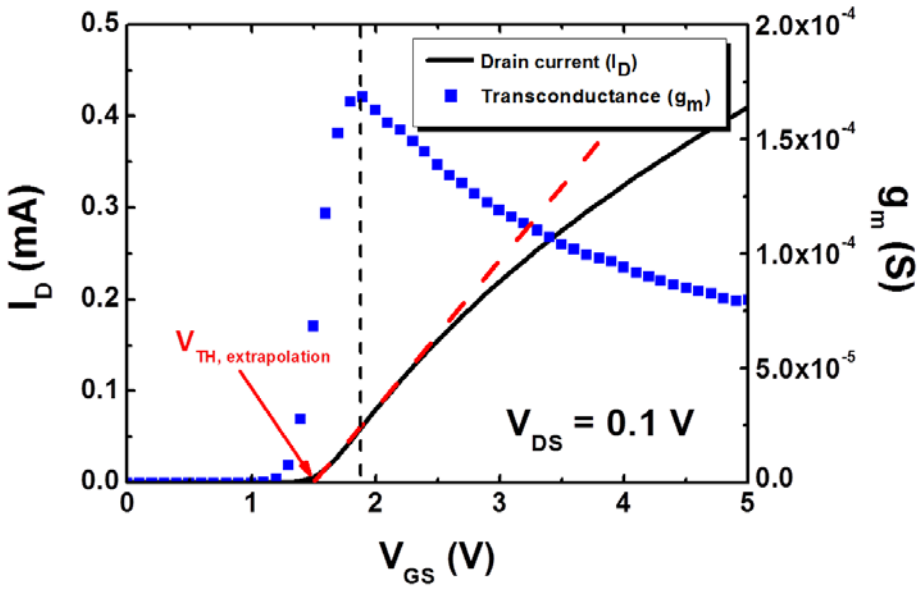


Figure 2.2 Illustration of the linear extrapolation method for a commercial n-channel MOS transistor (HCF4007UB, a dual complementary pair plus inverter comprised of three *n*-channel and three *p*-channel enhancement type MOS transistors) at V_{DS} = 0.1 V.

$$I_D = \frac{W}{L}\mu_{eff} C_{OX}\left(V_{GS} - V_{TH}\right)V_{DS} \tag{2.6}$$

At a constant of V_{DS}, based on Equation 2.6, the current expects to appear a linear curve for I_D-V_{GS} characteristic but the actual curve is not linear because the effective mobility will be degraded at higher gate voltage. Therefore, a point to fit Equation 2.6 is the point where the transconductance g_m (=dI_D/dV_{GS}) reaches its maximum value. The threshold voltage can be found at the point of zero current in the linear fit drawn with the I_D-V_{GS} curves focusing on the gate voltage at the $g_{m, max}$ as illustrated in Figure 2.2. However, the linear extrapolation method is sensitive to the series resistance and mobility degradation.

2.2.2 Second derivative method

The second derivative method (also named transconductance change or transconductance derivative) defines the threshold voltage with a secondly derivative curve (=d^2I_D/dV_{GS}^2) of the transconductance at small drain voltage ($V_{DS} < kT/q$) [47]. In this method, the gate voltage at the maximum value of the second derivative transconductance indicates the threshold voltage. The maximum point is related to the classical threshold band-bending of $\phi_S = \phi_F + V_{SB}$ that is the surface inversion layer being equal to the substrate doping (where V_{SB} is the source-substrate voltage) [48]. The transconductance derivative method is rather simple and more

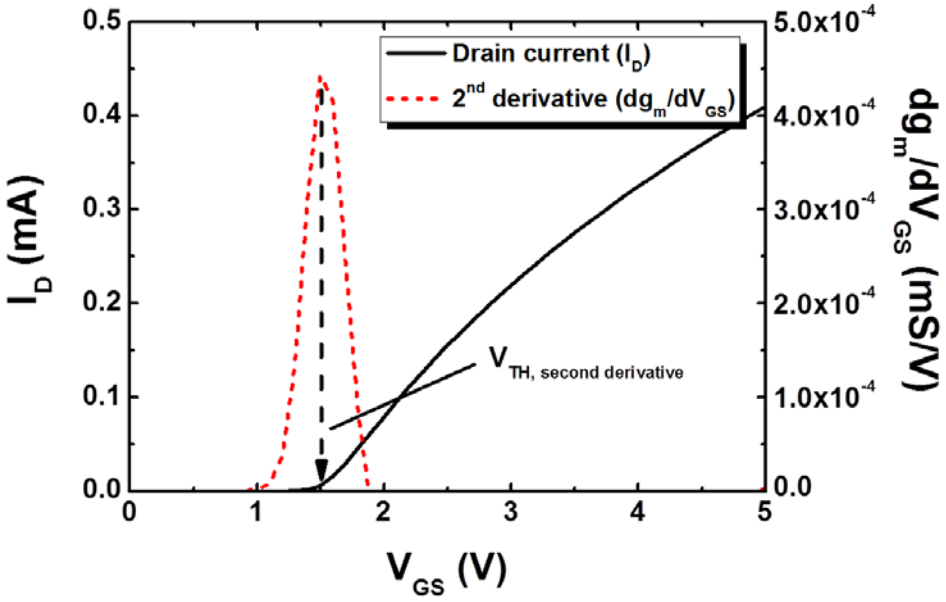


Figure 2.3 Illustration of second derivative method for a commercial n-channel MOS transistor (HCF4007UB) at V_{DS} = 0.1 V.

precise compared with linear extrapolation technique and less affected by the series resistance and mobility degradation.

2.2.3 Y-function method

The Y-function method (also called “drain current ratio” or “square root transconductance” method) was proposed by G. Ghibaudo in 1988 by combining the model of I_D-V_{GS} and g_m-V_{GS} characteristics to avoid the mobility degradation and the parasitic series resistance [46]. The model starts to consider the device in the linear operation at low drain voltage and the drain current can be expressed as Equation 2.6. Considering the dependence of the mobility on the gate voltage, it is represented as

$$I_D = \frac{WC_{OX}}{L}\frac{\mu_0}{\left[1+\theta_1(V_{GS}-V_{TH})\right]}(V_{GS}-V_{TH})V_{DS} \tag{2.7}$$

where μ_0 is the low field mobility, and θ_1 the mobility attenuation coefficient. Therefore, the transconductance of Equation 2.7 is

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L}C_{OX}\frac{\mu_0}{\left[1+\theta_1(V_{GS}-V_{TH})\right]^2}V_{DS} \tag{2.8}$$

The idea of Y-function method is the cancelation of the mobility attenuation coefficient θ_1 by dividing the current I_D with the square root of the transconductance g_m so that it results in

$$\frac{I_D}{g_m^{1/2}} = \left(\frac{W}{L} C_{OX} \mu_0 V_{DS}\right)^{1/2} (V_{GS} - V_{TH}) \tag{2.9}$$

In Equation 2.9, $I_D/g_m^{1/2}$ should be linear as increasing gate voltage with the intercept and slope which indicate the threshold voltage V_{TH} and low field mobility μ_0, respectively (Figure 2.4 (a)). After V_{TH} extraction, the mobility attenuation coefficient θ_1 can be also presented as shown in Figure 2.4 (b) using an expression which is given by

$$\theta_1 = [I_D / (g_m (V_{GS} - V_{TH})) - 1] / (V_{GS} - V_{TH}) \tag{2.10}$$

or it can be simplified as

$$\theta_1 = \frac{G_m}{I_D} - \frac{1}{V_{GS} - V_{TH}} \tag{2.11}$$

where G_m is defined as $W/L(C_{OX} \cdot \mu_0 \cdot V_{DS})$.

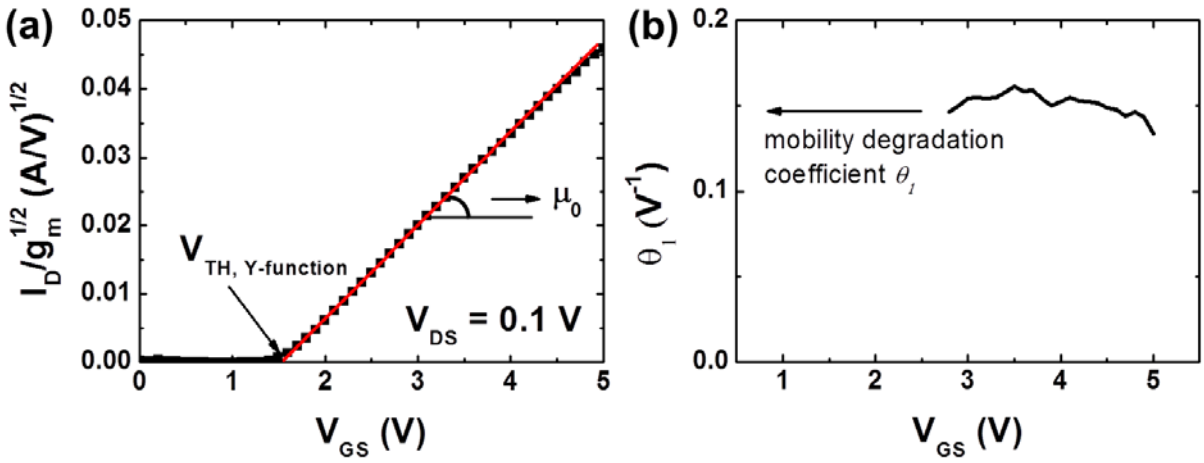


Figure 2.4 (a) $I_D/g_m^{1/2} - V_{GS}$ characteristic in a commercial n-channel MOS transistor (HCF4007UB) with an excellent straight fitting line (red solid line) and (b) extracted mobility attenuation coefficient θ_1 from Y-function method.

2.3 Carrier Mobility

In solid-state physics, the term 'carrier mobility' refers in general to the property of the carrier (electron or hole) to move in semiconductor (or metal) under an electric field ***E***. It can be also called an electron or hole mobility according to the carrier type but the term 'mobility' is more popular for all cases. When an electric field ***E*** is applied across the conductor, electrons (or holes) begin to move with an average velocity which is named the drift velocity $\boldsymbol{v_d}$. So, the electron mobility μ is defined as

$$\mathbf{v_d} = \mu\mathbf{E} \tag{2.12}$$

and it is specified in unit of cm^2/Vs. In an intrinsic semiconductor, the mobility is dependent on carrier scatterings by phonons, impurities, defects, or alloy disorder which affects the drift velocity. The approximate relationship between the mobility and scattering time is

$$\mu = \frac{q\tau}{m^*} \tag{2.13}$$

where q is the electronic charge, m^* the effective mass of a carrier in the semiconductor, and τ the average carrier scattering time. If the average scattering time τ_i for each scattering mechanism is independent, the total mobility due to several scatterings can be expressed using the Mathiessen rule given by [49]

$$\frac{1}{\mu} = \sum_i \frac{1}{\mu_i} \tag{2.14}$$

where μ_i ($=q\tau_i/m^*$) is the limited mobility with the different scattering time. The Matthiessen rule has been used to study the influence of various scattering on the mobility in MOSFETs as shown in Figure 2.5 [50].

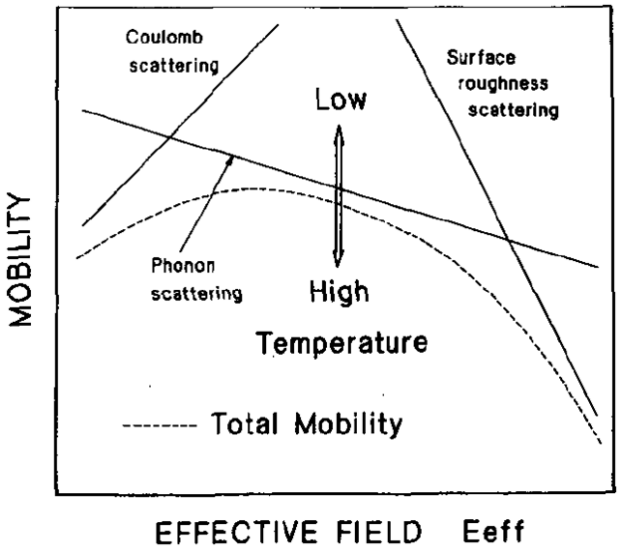


Figure 2.5 Schematic diagram of the effective field dependence of mobility in inversion layer by three dominant scattering mechanisms [50].

In semiconductors, the most common scattering mechanisms are ionized impurity scattering and phonon scattering (precisely, acoustic phonon scattering). The ionized impurity scattering is especially important for highly doped semiconductors and it stands for the carrier scattering by influencing the electric field of the ionized impurities coming from donors and/or acceptors in semiconductors. The scattering potential of ionized impurity scattering is assumed similar to Coulombic scattering but the ionized impurity scattering attracts mobile carriers which screen the potential. For the phonon (or lattice) scattering, the semiconductor's band structure is influenced by changes in lattice spacing at any temperature above 0 K. The vibration of atoms causing the lattice spacing creates pressure (acoustic) waves in crystal, which are called phonons inducing the carrier scattering. There are two kinds of phonons: one is the acoustic phonons

and the other is optical phonons. The acoustic phonons are the lattice spacing due to the displacement of neighboring atoms in the same direction whereas the optical phonons coming from the opposite directions [51]. Apart from these major scattering mechanisms in semiconductors, there are also other important scatterings such as neutral impurity scattering, surface roughness scattering, and defect scattering depending on materials, structures, and process.

There are several mobilities in use depending on the extraction method. Representatively, they are conductivity mobility, Hall mobility, and MOSFET mobility for the characterization of semiconducting materials and devices.

2.3.1 Conductivity (or drift) carrier mobility

The conductivity mobility (μ_{drift}) is derived from the simple relation between mobility and electrical conductivity σ that is the proportional to the product of the mobility and carrier concentration in semiconductor materials. The conductivity is given by

$$\sigma = q(n\mu_{drift,e} + p\mu_{drift,h}) \tag{2.15}$$

where n is the electron density, $\mu_{drift,e}$ the electron mobility, p the hole density, and $\mu_{drift,h}$ the hole mobility. The conductivity mobility is simple and easy to find but the majority carrier density is needed to obtain the accurate conductivity mobility. It is useful to characterize for the intrinsic property of materials.

2.3.2 Hall carrier mobility

The Hall measurement is a well-common method based on Hall Effect to obtain the mobility, carrier type, and carrier concentration in material. The Hall Effect is a phenomenon to produce a potential difference (Hall voltage, V_H) perpendicular to the magnetic field and current when the magnetic field applied to the electrical conductor perpendicular to the current flow direction. As shown in Figure 2.6, it shows a schematic illustration of Hall Effect in a p-type conductor and the force causing Hall voltage is given by the vector expression

$$\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B}) \tag{2.16}$$

and Hall mobility μ_H is defined by

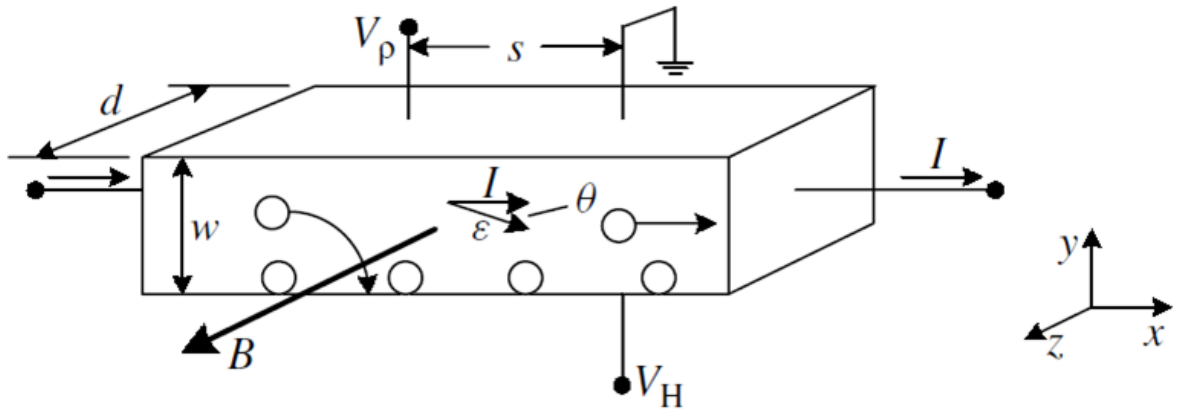


Figure 2.6 Schematic illustration of the Hall Effect in a *p*-type conductor [47].

$$\mu_H = \frac{|R_H|}{\rho} = \frac{dV_H}{\rho BI} \tag{2.17}$$

where R_H is the Hall coefficient, B the magnetic field, I the current, and ρ the resistivity. The Hall mobility is trustworthy compared with the conductivity mobility but the method requires the sample having appropriate geometries for Hall measurement.

2.3.3 MOSFET carrier mobility

In general, the conductivity and Hall mobilities are for bulk. In the case of MOSFETs, the surface is relatively important and the mobility is easily affected by various scatterings such as ionized impurity scattering, phonon scattering, and so on. Considering these scatterings, the total mobility is limited by the lowest mobility according to Mathiessen's rule. Therefore the method to extract the mobility only for MOSFET structures has been used. Effective mobility and Field-effect mobility are well-known terminology widely used for various material devices as well as silicon MOSFETs. Let consider an n-channel MOSFET of gate length L and width W. The drain current is simplified for the basic MOSFET operation as

$$I_D = g_d \cdot V_{DS} = \frac{W}{L}\mu_{eff} Q_i V_{DS} \tag{2.18}$$

where g_d is the drain conductance, μ_{eff} the effective mobility and Q_i the inversion channel charge density (C/cm^2). To extract the exact value of effective mobility, the inversion charge density Q_i is important and it can be determined in two different ways. One is a simple approximation with

$$Q_i = C_{OX}(V_{GS} - V_{TH}) \tag{2.19}$$

and the other is a direct measurement of Q_i from the capacitance measurement (refer Chapter 2.6). The direct measurement of charge carriers is better than the approximation to extract the value of effective mobility. However, it is not convenient in many ways such as a necessity of additional *C-V* measurement and several capacitance effects (e.g. an overlap capacitance) depending on the device structure. For this reason, the approximation method is well used for the comparison for the number of devices and the capacitance measurement is recommended to obtain the more precise value of mobility.

For the effective mobility, the drain voltage is typically recommended about 50~100 mV as small as possible considering the uniformity of inversion charge carriers from source to drain. The definition of effective mobility is given by

$$\mu_{eff} = \frac{g_d L}{W Q_i} \tag{2.20}$$

and the drain conductance g_d is defined as

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=cons\tan t} \tag{2.21}$$

The ionized impurity scattering and surface roughness scattering that mainly affects the effective mobility depends on the substrate doping concentration and the electric field. The relation between the effective mobility and the surface electric field can be expressed as

$$\mu_{eff} = \frac{\mu_0}{1 + \left(\alpha E_{eff}\right)^{\gamma}} \tag{2.22}$$

where α and γ are constants. In Equation 2.22, the “universal” mobility curves for the electric field which can be expressed as the electric field due to the space-charge region and the inversion layer charges [52-54]. But, the universal mobility is not good for understanding the device operation because the gate voltage can be measured experimentally, not the electric field. Therefore, the empirical relationship for the effective mobility degradation for the gate voltage is [55]

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1(V_{GS} - V_{TH}) + \theta_2(V_{GS} - V_{TH})^2} \tag{2.23}$$

where θ_1 and θ_2 are mobility attenuation factors which are related to the series resistance and surface roughness, respectively [56]. In the long channel devices, the value of θ_2 is negligible but, in the case of short channel, it may significantly affect to the mobility.

On the other hands, the field-effect mobility is determined using the transconductance g_m contrary to the effective mobility for the drain conductance g_d which is given by

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=constant} \tag{2.24}$$

and the field-effect mobility is defined as

$$\mu_{FE} = \frac{Lg_m}{WC_{OX}V_{DS}} \tag{2.25}$$

The effective and field-effect mobility are widely used with little consideration for nano devices analysis. However, it is noted that there is mathematically a distinct difference for considering electric field dependence on the mobility. Figure 2.7 shows for the effective and field-effect mobility as a function of the gate voltage. The effective mobility is much larger than the field-effect mobility. It is due to the disregard of the electric field dependence for the mobility in the derivation of Equation 2.25 [57].

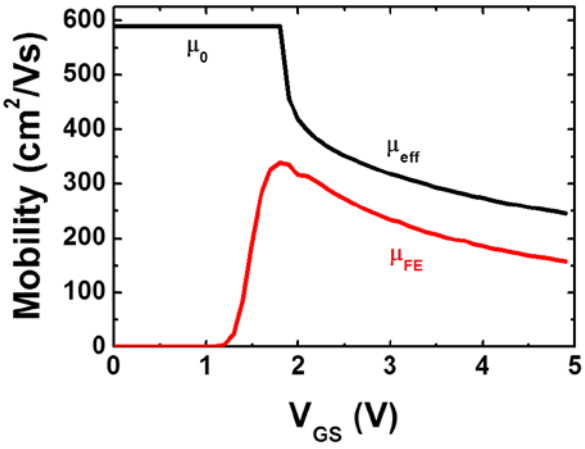


Figure 2.7 Comparison of the effective and field-effect mobilities (HCF4007UB).

2.4 Series and contact resistances

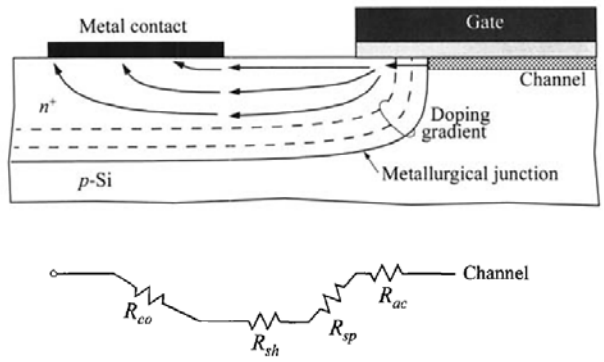


Figure 2.8 Different components of parasitic S/D series resistance. (R_{ac} is the accumulated-layer resistance due to doping gradient, R_{sp} the spreading resistance, R_{sh} the sheet resistance, and R_{co} the contact resistance) [59].

The term "series resistance" refers to the additional resistance which contributes to the total resistance of the device. It comes from the electrical connections from leads and contacts. It could be called "contact resistance" but it has been used for the metal-semiconductor junction as a main contribution [58]. Firstly, the series resistance in CMOS technology stands for the parasitic source/drain (S/D) resistance connected to the channel in series when the device size is decreased. Therefore, the series resistance has been often understood the parasitic resistance. Figure 2.8 illustrates the detailed

schematic and the circuit model for different parasitic series resistances [59]. However, the resistance between source and drain is mostly classified as the source resistance R_S, the drain resistance R_D, the channel resistance R_{ch}, and the contact resistance R_C for the analysis. For MOSFETs, the total resistance R_{total} can be expressed a summation of R_{ch} and R_{SD} (=R_S+R_D) as

$$\begin{aligned} R_{total} &= R_{ch}(V_{GS} - V_{TH}) + R_{SD} \\ &= \frac{L}{W}\rho_{ch}(V_{GS} - V_{TH}) + R_{SD} \end{aligned} \tag{2.26}$$

where ρ_{ch} is the resistivity of the channel. The series resistance R_{SD} can be extracted from the mobility attenuation factor θ_1 based on Y-function method [60],

$$\theta_1 \equiv \frac{G_m}{I_D} - \frac{1}{(V_{GS} - V_{TH})} = \theta_{1,0} + \beta(R_S + R_D) \tag{2.27}$$

$$\beta = \frac{W}{L_{eff}} C_{OX}\mu_0 \tag{2.28}$$

Using Equation 2.27 and 2.28, θ_1 can be drawn as a linear function of β which is shown in Figure 2.9. The slope and the intercept with y axis of the plot gives the values of the total series resistance R_{SD} and the intrinsic mobility attenuation factor $\theta_{1,0}$, respectively. Interestingly, R_{SD} extraction is not affected by L_{eff} variations or L_{eff}-dependent μ_0 variations.

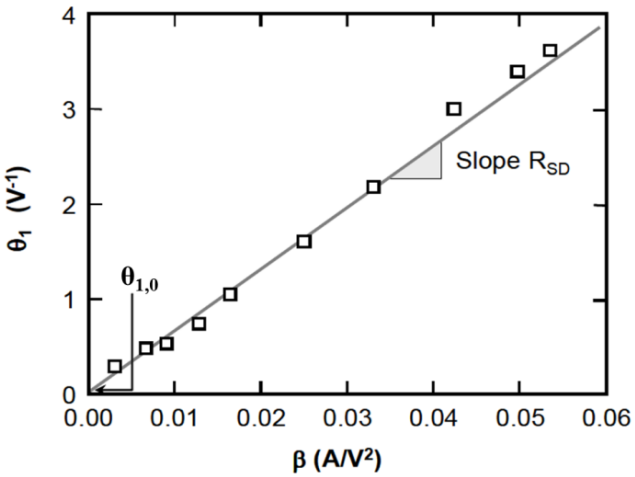


Figure 2.9 Extraction of the series resistance R_{SD} and mobility attenuation factor θ_1 [60].

There is another resistance which called contact resistance mainly observed in the metal-semiconductor junctions. In 1874, F. Braun firstly reported the asymmetrical conduction between metal points and crystals [61]. The rectifying properties of the metal-semiconductor contact arise from the existence of an electrostatic barrier so called “Schottky barrier” at the interface between the metal and semiconductor. Theoretically, the electrostatic barrier is due to the difference in work functions of two materials (Figure 2.10). If the barrier height is small, the junction makes an “Ohmic” contact that presents a linear curve in current-voltage relationship. However, for the large barrier height, it is called “Schottky” contact due to the rectifying

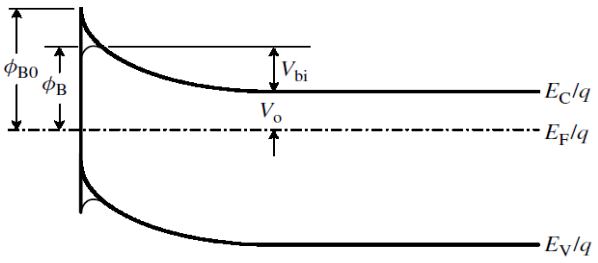


Figure 2.10 Energy band diagram of the Schottky barrier [47].

behaviors. The Schottky barrier is frequently observed in nanowire or nanotube devices with bottom-up grown nanostructures and it is one of the important issues for nanowire applications. The conduction mechanisms in metal-semiconductor are illustrated in Figure 2.11: thermionic emission (TE), thermionic-field emission (TFE), and field emission (FE) [59]. For the evaluation of contact resistance, several methods are employed presently, such as transmission-line method (TLM), gated four-prove measurement, modified time-of-flight method, Kelvin probe force microscopy (KFM) and electric-field induced second harmonic generation (SHG) method [62-66].

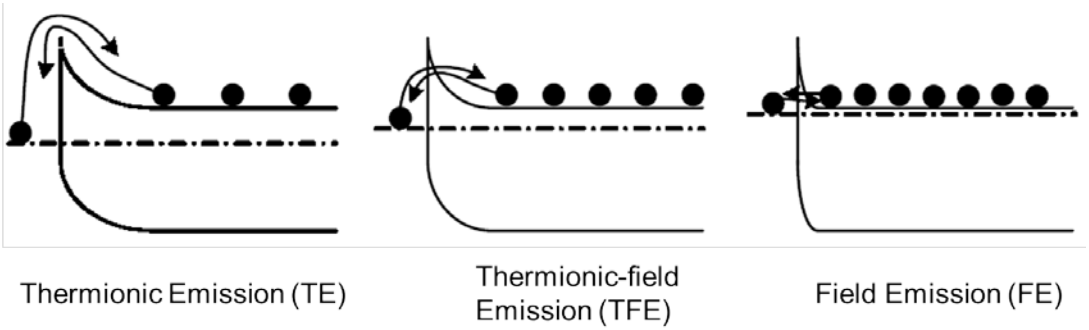


Figure 2.11 Different conduction mechanisms in metal-semiconductor contacts: thermionic emission (TE), thermionic-field emission (TFE), and field emission (FE) [47].

2.5 Subthreshold swing

In a MOSFET, a small current exists between the source and the drain when the gate bias is below threshold voltage and the semiconductor surface is in weak inversion (i.e. subthreshold region). The current in the subthreshold region is named subthreshold current or a subthreshold leakage. Its behavior is similar to the exponentially increasing current of a forward biased diode because the subthreshold current is dominated by the diffusion current and not the drift current owing to lower electron charge in the channel [59]. In the subthreshold region (below threshold), the drain current of a MOSFET in all region can be expressed [67]

$$I_D = I_{D1} \exp\left(\frac{q(V_{GS} - V_{TH})}{nkT}\right)\left(1 - \exp\left(-\frac{qV_{DS}}{kT}\right)\right) \tag{2.29}$$

where I_{D1} depends on temperature, device dimensions, and substrate doping density and n is given by n=1+(C_b+C_{it})/C_{OX} where C_b, C_{it}, and C_{OX} are respectively bulk, interface trap, and oxide capacitance per unit area. The subthreshold swing can be obtained from the plot of log (I_D) versus V_{GS} when V_{DS} is much larger than thermal voltage (i.e. V_{DS} >> kT/q). As shown in Figure 2.12, the subthreshold swing is expressed as the reciprocal of slope in linear region. It corresponds to the gate voltage necessary to increase the drain current by one decade. Therefore, the subthreshold swing is given by

$$S = \frac{1}{Slope} = \frac{\ln(10)nkT}{q} \approx \frac{60nT}{300} mV / decade \tag{2.30}$$

The subthreshold swing is known to have minimum theoretical limit of 59.6 mV/decade (S=ln(10)kT/q) in the case of very thin Si-SiO_2 interface having no traps at room temperature [68]. It is one of the fundamental issues for silicon based MOSFET scaling since the subthreshold swing is increased as decreasing the channel length. The subthreshold swing is related to logic circuits for low-power, high-speed applications and it is an important parameter to determine the device performance for the MOSFET miniaturization [69].

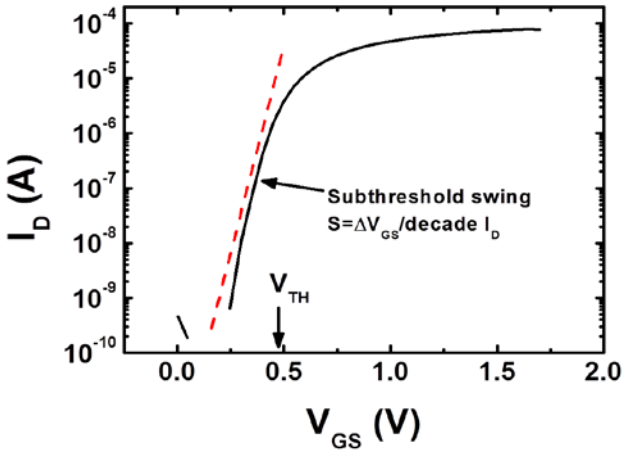


Figure 2.12 Log (I_D) versus V_{GS} of 3-D stacked gate-all-around (GAA) silicon nanowire transistor.

2.6 Capacitance

The capacitance-voltage (C-V) measurement is one of the most useful and common method to characterize electrical properties of materials and their interfaces. The C-V measurement is a specific technique for the impedance spectroscopy that has been used to investigate charge carriers in the bulk or interfacial region of any kind of solid or liquid material: ionic, semiconductor, mixed electronic-ionic, and dielectrics [70]. In MOSFETs, it has been mainly used to characterize oxide thickness, doping concentration, flat-band voltage, oxide charge, work function, and interface state density in MOS devices [47]. The

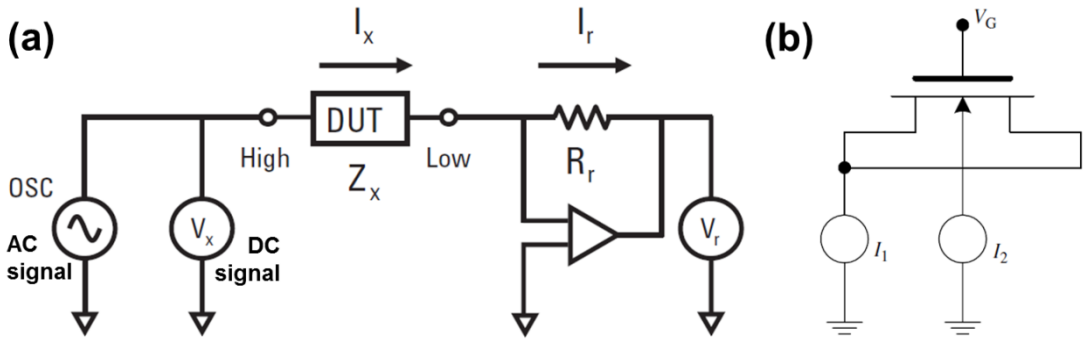


Figure 2.13 (a) Schematic diagram of an impedance measurement method named auto-balancing bridge method [73] and (b) Split C-V measurement arrangement [47].

capacitance is determined with the width of space-charge (i.e. depletion) region in a semiconductor junction applying small amplitude of AC voltage (or current) on a DC voltage. Typically, the frequency of AC signal is used with 10 kHz to 1 MHz and the amplitude is recommended as small as possible for accurate measurements or near the thermal voltage (≈ 25 mV) [71], [72]. But, the amplitude is used from 10 to 50 mV practically and it is adjustable depending on the devices.

Figure 2.13 (a) shows a schematic of the impedance measurement method called an auto-balancing bridge method which is adapted to conventional equipment systems [73]. To measure capacitance in MOSFETs, the most widely used *C-V* measurement technique is called "split *C-V*" technique and consists in measuring the capacitance of the gate to channel (source/drain) and the gate to substrate as illustrated in Figure 2.13 (b) [74]. A time-varying gate voltage gives rise to currents I_1 and I_2. With the substrate grounded, the channel inversion charge density C_i and the substrate depletion charge density C_b can be derived from I_1 and I_2 which is given by

$$I_1 = \frac{dQ_i}{dV_{GS}}\frac{dV_{GS}}{dt} = C_i\frac{dV_{GS}}{dt} = C_{GC}\frac{dV_{GS}}{dt} \tag{2.31}$$

$$I_2 = \frac{dQ_b}{dV_{GS}}\frac{dV_{GS}}{dt} = C_b\frac{dV_{GS}}{dt} = C_{GB}\frac{dV_{GS}}{dt} \tag{2.32}$$

where C_{GC} is the gate-to-channel and C_{GB} the gate-to-bulk capacitance per unit area. Figure 2.14 shows the capacitance behavior of C_{GC} and C_{GB} from the split *C-V* measurements. The inversion charge Q_i and the substrate depletion charge Q_b can be obtained by the integration of C_{GC} from the accumulation to the gate voltage and C_{GB} from the flat band voltage to the inversion, respectively. The expressions for Q_i and Q_b are given by

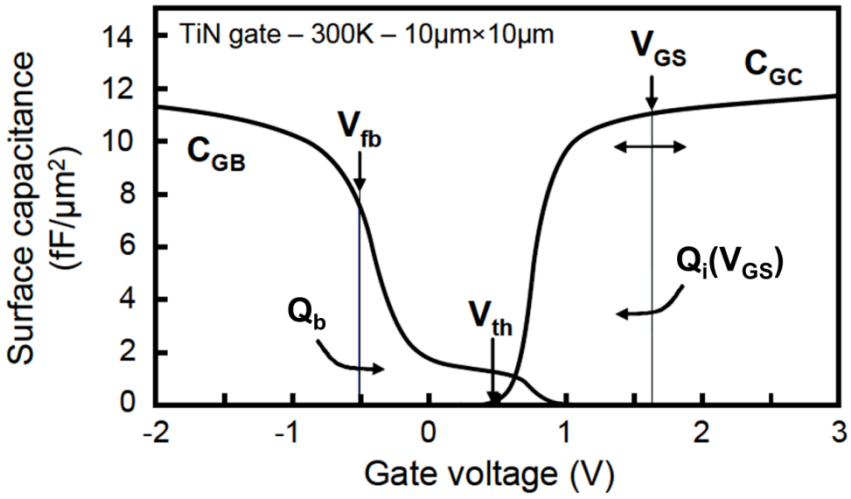


Figure 2.14 C_{GC} and C_{GB} behaviors as changing the gate voltage and principle of Q_i and Q_b with split *C-V* measurements [60].

$$Q_i = \int_{V_{acc}}^{V_{GS}} C_{GC} dV_{GS} \tag{2.33}$$

$$Q_b = \int_{V_{FB}}^{V_{inv}} C_{GB} dV_{GS} \tag{2.34}$$

With the results of Equation 2.33 and 2.34, the effective mobility and effective field can be calculated as [60]

$$\mu_{eff}(V_{GS}) = \frac{L}{W} \frac{I_D(V_{GS})/V_{DS}}{Q_i(V_{GS})} \tag{2.35}$$

$$E_{eff}(V_{GS}) = \frac{|Q_b| + \eta |Q_i(V_{GS})|}{\varepsilon_{ch}} \tag{2.36}$$

where ε_{ch} is the permittivity of channel material and η the empirical weighting parameter, which is varying with device type, doping concentration and temperature [75], [76].

2.7 Summary

In this chapter, the major device parameters to understand the transport properties based on the classical MOS transistor model were summarized together with the practical extraction methods. These parameters such as threshold voltage, mobility, series resistance, subthreshold swing, and capacitance are also useful to describe the electrical operation of nano-scale devices considering some fitting procedures. The parameter extractions and their

physical meanings can help to understand the physical phenomena and optimize the materials and fabrication processes correlated to the efficiency of carrier transport.

Chapter 3 Low-frequency noise characterization

3.1 Background: Definition and concepts

In general, noise refers to any unwanted signal that is commonly observed in signals such as sounds, electronics, images, communications, and so on. For example, in communication systems, the noise signal blocks, changes, interferes or distorts the original messages and thereby the message may not deliver its meaning accurately. Similarly, noise also exists in all electronic devices and circuits as a result of the randomly spontaneous perturbation in the current (or voltage) due to the random movement of charge carriers and carrier fluctuations in the semiconductors by several reasons such as temperature, defects, and etc. The noise in electronic systems has been called “electronic noise”.

The electronic noise can be briefly classified into two types: one is an external noise which is defined as a noise from other outer noise sources such as light, sound, and vibration and not from the electronic device itself. The external noise which is easy to observe in electrical measurements is the hindrance for understanding the inherent noise in electronic devices. However, it can be reduced or removed by some appropriate shielding techniques. In spite of the minimization of the external noise, on the other hand, there is still a noise due to an electronic device or rather a material itself like a semiconductor. It is named an internal noise as a unique property of the electronic device. Accordingly, the internal noise cannot be entirely eliminated unlike the external noise but it can be effectively reduced by proper manufacturing process and design for the devices and circuits. In general, the study of electronic noise in solid-state devices reveals internal noise which explains the phenomena of current fluctuations following in the semiconductor. Figure 3.1 shows an example of drain current signal fluctuations with different structures of MOSFETs [77].

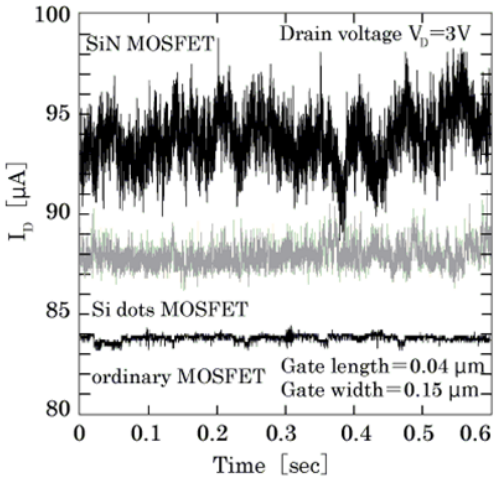


Figure 3.1 Drain current signal fluctuations in time domain [77].

In detail, the time varying current *I(t)* in the semiconductor, considering the electronic noise, can be expressed as

$$I(t) = I_0 + i(t) \tag{3.1}$$

where I_0 is the average value of current for a certain applied voltage and *i(t)* is the small-signal variables of the randomly fluctuated currents in time variation. Since *i(t)* is a random variable, it cannot be predicted at any point in time. To characterize the noise in current signal *I(t)*, one typical way is the averaging of random signals. By definition, however, the noise is non-deterministic as previously mentioned so that it is difficult to obtain a proper mean value and cannot be represented by any mathematical function. Indeed, the average of current *I(t)* which is measured for a certain time period will be always zero. For this reason, another mathematical quantity is required to properly represent the random noise behaviors in the current. In general, there are several squared quantities and one of them named the power spectral density (PSD) *S*(*f*) is generally used which is given by a Fourier transform method. A Fourier transform method is a well-known and powerful technique for the effective noise analysis which converts the random variables in the time domain to the frequency domain and it is defined as

$$X(f) = \int_{-\infty}^{\infty} x(t) e^{-j2\pi ft} dt \;\Leftrightarrow\; x(t) = \int_{-\infty}^{\infty} X(f) e^{j2\pi ft} df \tag{3.2}$$

where *X*(*f*) is the Fourier transform and *x*(*t*) is the inverse Fourier transform. If the Fourier transform decomposes the random signal into its constituent frequencies, the noise can be written as the sum of simple waves mathematically represented by sine and cosine. However, the Fourier transform is not desirable for all kinds of random signal because there is no inverse Fourier transforms for the conversion. To solve such mathematical problem in the Fourier transform, the autocorrelation function *R(s)*, which is same process compared to the Fourier transform according to the Winer-Khintchine theorem, has been used [78], [79]. So, the PSD is given by

$$S(f) = 4\int_0^{\infty} R(s)\cos(2\pi fs) ds \tag{3.3}$$

and it reflects how the noise power is distributed with frequency. The PSD can be obtained with a spectrum analyzer and the unit of PSD generally used in A^2/Hz and V^2/Hz for the noise current (S_I) and noise voltage (S_V), respectively.

Noise characterization has been one of the useful techniques to characterize the device reliability and the failure analysis for typical microelectronic devices because the noise forms an intrinsic lower noise limit and depends on material and fabrication processing [47].

Moreover, the noise spectroscopy has been applied to the study of deep levels in MOSFET like a deep-level transient spectroscopy (DLTS) [80]. Even the noise spectroscopy can be applied to very small area devices whereas the DLTS is impossible. Especially, for nano scale devices, the noise should be considered because it increases relatively as decreasing the current level due to the smaller size of device. Therefore the noise is getting important for low-dimensional structures. Why the electronic noise is important for nano scale devices? Basically, the resolution limit of an electronic device (e.g. a sensor) for the signal detection is determined by the signal to noise ratio (SNR). If the device has high signal level (i.e. high current), the resolution for the signal detection is generally limited by the electronic circuits whereas it becomes more sensitive to noise when the device has smaller current level. As a result, the noise restricts the minimum value of the input signal that determines the output signal of electronic circuits.

3.2 Fundamental noise sources

In the view point of physics, the electronic noise is one of carrier dynamics which is correlated to the scattering process in a solid-state. The scattering process is due to some collisions of charge carriers because of lattice vibrations during the transport or trapping/de-trapping of charge carriers on the trap sites. It has been known that the scattering elements are channel defects, interface states, oxide traps or contacts. There are various kinds of noise sources and it represents different behaviors in the frequency domain depending on the noise source. In this chapter, the representative fundamental noise sources are discussed and described.

3.2.1 Thermal noise

Thermal noise (also called Johnson, Nyquist, or white noise) is caused by the random thermal motion of current carriers (i.e. electrons or holes) in a semiconductor. In 1906, A. Einstein predicted that Brownian motion of charge carriers would lead to fluctuations in the potential across a resistor in thermal equilibrium [81]. Later on, in 1928, J. Johnson firstly measured [82] and H. Nyquist theoretically explained it [83]. Thermal noise is always presented for every semiconductor in the absence of an electrical field to be applied. The PSD of thermal noise is constant over a frequency range, which is why it is called white noise. The

voltage PSD of thermal noise due to the Brownian motion of carriers can be expressed as

$$S_V = 4kTR \tag{3.4}$$

where k is the Boltzmann constant, T the absolute temperature, and R the resistance. The corresponding current PSD of thermal noise is given by

$$S_I = \frac{S_V}{R^2} = \frac{4kT}{R} \tag{3.5}$$

Thermal noise always exist (except T=0 K) thereby it is frequently used for comparison between other noise types and thermometry purposes which provides the resistance R. For example, thermal noise is often used to calibrate a noise measurement system because it can give some value for the limits of the noise measurement system with temperature [84].

3.2.2 Shot noise

Shot noise has been known as the discrete nature of charge transport. It is generally observed in devices having a potential barrier such as *pn* junctions, and Schottky diodes. In 1918, W. Schottky firstly discovered in vacuum tubes and derived an equation shown as the Schottky formula [85]. The PSD of shot noise is proportional to the electronic charge q of the carriers and the mean current I,

$$S_I = 2qI \tag{3.6}$$

There is no expression for the voltage PSD in shot noise because the current is necessary for the generation of shot noise. The shot noise is also called a white noise like thermal noise because its frequency dependence is the same as thermal noise. Thus, it cannot be distinguished simply due to the existence of the thermal noise. But the shot noise is generally much smaller than the thermal noise. Recently, shot noise becomes important in mesoscopic systems because the size of a mesoscopic system is comparable to some typical lengths which determine the level of electron correlations and the shot noise is correlated to the system length [86].

3.2.3 Generation-Recombination (g-r) noise

Generation-recombination (g-r) noise is due to generation and recombination of charge carriers (i.e. electrons or holes) by trap sites which induce the conductance (or resistance) fluctuations. In semiconductors, the localized state cannot participate to the conduction

whereas the delocalized states contribute to the electron conduction. These localize states also named “traps” exist due to the presence of various defects or impurities in the semiconductor or at the interface. The PSD of g-r noise is given by a Lorentzian behavior

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{S_N}{N^2} = \frac{\overline{\Delta N^2}}{N^2}\left[\frac{4\tau}{1+(2\pi f\tau)^2}\right] \tag{3.7}$$

where N is the averaging number of free carriers, $\overline{\Delta N^2}$ the variance of the fluctuating number of charge carriers, and τ the carrier relaxation time. The relaxation time τ is in the range of 10^{-6} s to 10^{-3} s as a characteristic of traps. The g-r noise is only valid when the Fermi energy level is near, within a few kT, to the trap energy level [87]. In general, the trap characteristics depend on the trap energy level and spatial position.

3.2.4 Random-Telegraph-Signal noise

Figure 3.2 illustrates a schematic description of RTS noise in a MOS structure and the current waveform in time domain. Random-Telegraph-Signal (RTS) noise (also called burst noise, popcorn noise, impulse noise, and bi-stable noise) is an unusual case of g-r noise involving only few traps. The level of current will be between two or more states due to the random trapping and de-trapping of charge carriers. A simple two-level RTS noise can be observed in various types of semiconductor devices. Especially, RTS noise is common in

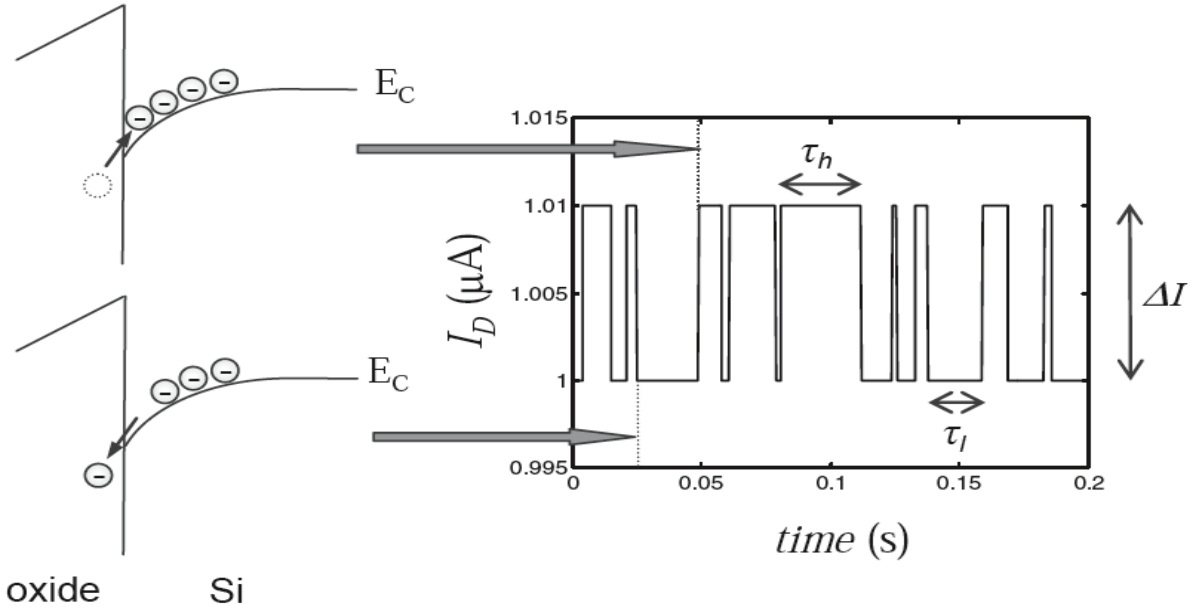


Figure 3.2 Schematic description of RTS noise in a MOS structure and a waveform of current in time domain [87].

small area MOS transistors and is correlated to individual carrier trapping at the silicon-oxide interface [88-90]. Likewise g-r noise, the PSD of RTS noise is a Lorentzian type and derived as

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_l + \tau_h)[(1/\tau_l + 1/\tau_h)^2 + (2\pi f)^2]} \tag{3.8}$$

where τ_l and τ_h are the time constant in the lower state and higher state, respectively and ΔI is the difference of current between those two states (Figure 3.2). This type of noise is a good for study of a single trap activity in a system with few free carriers.

3.2.5 1/*f* noise

1/*f* noise is generally also named flicker or excess noise with a PSD inversely proportional to the frequency *f*. It has been sometimes called low-frequency noise but it is not true strictly because other types of noise such as g-r or RTS noise can be observed in low-frequency region. Nevertheless, it is accepted since most of noise type is 1/*f* noise. In 1925, the 1/*f* noise was firstly found by J. Johnson in vacuum tubes and Schottky gave the first interpretation [91]. Since then, Christensen & Pearson found it for carbon microphones in 1936 and then the 1/*f* noise was also found in various semiconductor and semiconductor devices [92]. Up to now, a huge number of current noise spectra were measured with various materials such as semiconductors, semimetals, metals, superconductors, tunnel junctions, strongly disordered conductors, and etc. thereby the results, in practically all cases, appeared in a shape of an increase of current noise power spectrum as decreasing the frequency, 1/*f*. In general, 1/*f* noise is difficult to find at high frequency since it is finally hidden by thermal noise.

Even if 1/*f* noise is universal for various materials, there are still some controversies for the origin since many decades. Some major issues are as follows [93]: 1) Mobility vs. Number fluctuations, 2) Superposition of RTS noise for 1/*f* noise, and 3) Surface vs. Bulk origin.

1) Mobility vs. Number fluctuations: It is a well-known issue to understand the origin of 1/*f* noise. The current fluctuation in materials can be understood with the conductivity fluctuations since the conductivity is an inherent property which determines the device conductance. So, the conductivity σ is defined as

$$\sigma = qn\mu_{drift} \tag{3.9}$$

where n is the charge carrier density and μ_{drift} is the drift mobility. From the idea of conductance fluctuations, two representative models are presented. From a physical view point, the number fluctuation model is based on the charge trapping/release of carriers into the oxide or at the interface states whereas the mobility fluctuation model is due to phonon scattering in the solid [94]. In conventional MOSFETs, the main 1/*f* noise source has been generally explained by the number fluctuation model. But there are other devices where noise is explained by the mobility fluctuation model. For instance, for 0.35 μm *p*-type FETs, the mobility fluctuation model dominates in reason of the buried architecture of the channel [95]. On the other hand, some results support the mobility fluctuation [96], [97]. In carbon nanotubes, the number fluctuation with charge trapping at the interface does not work and the other explanation is suggested such as diffusion or electron-phonon interaction. The electron-phonon interaction is strongly supported by the result which is the temperature dependence of 1/*f* noise in single-walled carbon nanotubes [97]. These results show that the noise can be changed depending on the devices architecture or conduction mechanism.

2) Superposition of Lorentzian noise for 1/*f* noise

The idea of superposition of Lorentzian noise to obtain the 1/*f* behavior has been suggested by J. Bernamont [98] and M. Surdin [99]. The power spectra of g-r and RTS noise show Lorentzian curves, which are explained with the trap time constant [100-102]. If the traps having various time constants are independent, the superposition of Lorentzian curves looks like 1/*f* behavior as shown in Figure 3.3. The idea has been well explained in small area as well as in large area MOS devices. However, there are some criticisms that RTS noise is not a fundamental source of 1/*f* noise because 1/*f* noise still exists in the absence of the RTS noise.

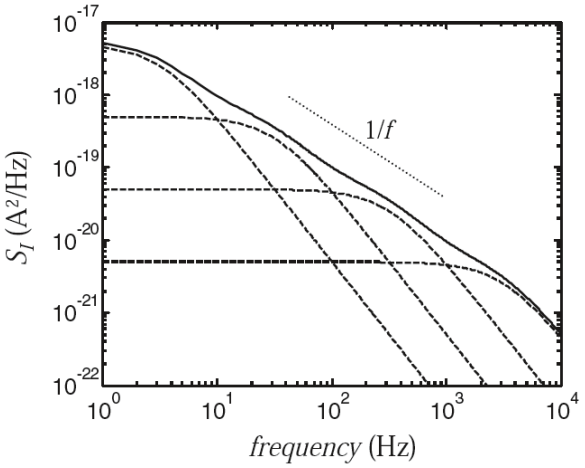


Figure 3.3 Superposition of several Lorentzians giving a 1/f noise.

3) Surface vs. Bulk origin

The arguments of the surface or bulk effect on the 1/*f* noise basically is coming from a controversy of the mobility and number fluctuation model. Two competing theories have been proposed: the McWhorter number fluctuation theory which considers the surface effect and the Hooge mobility fluctuation theory for homogeneous bulk such as metals and semiconductors [103]. Both theories are supported with experimental evidence. The general belief is surface or bulk noise or both of them depending on the device structures. In nanowire structures, the surface/volume ratio is increased as decreasing the channel diameter. It is noted that the surface effect due to the smaller size might be important for the 1/*f* noise behavior in nanowire structures.

3.3 1/*f* noise models for FET structures

3.3.1 Hooge mobility fluctuation model

The mobility fluctuation model is an empirical relation between the magnitude of the 1/f noise and the number of free charge carriers proposed by Hooge in 1972 [104]. It is simply given by

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{\alpha_H}{Nf} \tag{3.10}$$

where N is the total number of free carriers and α_H is dimensionless constant, called Hooge constant. At first, the Hooge constant has been known to be a universal constant having the value of 2×10^{-3} for all materials but it becomes known to be wrong later. Hooge proposed the model for homogeneous bulk systems. Later on, the Hooge mobility fluctuation model distinguished from the mobility fluctuations by the scatterings due to trapped charge carrier at the oxide-semiconductor interface. Physically, the Hooge mobility fluctuation model explained the 1/*f* noise is due to the current fluctuations resulting from the mobility scattering by phonon (or lattice) vibrations. Unfortunately, the Hooge model cannot provide a further explanation for the 1/*f* noise even though it is well fitted empirically. For the Hooge constant, it has been known that there is no physical meaning. Nevertheless, it has been used to compare the noise between different devices or materials.

I. Hafez et al. proposed the Hooge mobility fluctuation model for the Ohmic and non-linear region of MOSFETs [105] and it can be defined involving the total number of carriers is given by $N=WLQ_i/q$,

$$\frac{S_{Id}}{I_D{}^2} = \frac{q\alpha_H}{WLQ_i f} \tag{3.11}$$

where Q_i is the inversion charge per unit area. And the input gate voltage noise in Ohmic operation is

$$S_{Vg} = \frac{q\alpha_H}{WLC_{OX} f}(V_{GS} - V_{TH})\left[1 + \theta_1(V_{GS} - V_{TH})\right]^2 \tag{3.12}$$

where θ_1 is the mobility attenuation coefficient as shown in Equation 2.7. In the same manner, in non-linear region MOSFETs, the model can be expressed considering the non-uniform inversion layer along the channel as

$$\frac{S_{Id}}{I_D^2} = \frac{q\alpha_H}{fWL^2}\int_O^L \frac{dy}{Q_i(y)} = \frac{q\alpha_H}{fWL^2}\int_O^{V_{DS}} \frac{W\mu_{eff}}{I_D} d\phi_c = \frac{q\alpha_H < \mu_{eff} > V_D}{fL^2 I_D} \tag{3.13}$$

where $<\mu_{eff}>$ is the average mobility along the channel. Regardless of the Ohmic and non-linear regions of MOSFETs, the normalized drain current noise is inversely proportional to the drain current (i.e. $S_{Id}/I_D{}^2 \sim 1/I_D$).

3.3.2 Carrier number fluctuation model

In 1957, in MOS structures, the original theory for number fluctuations that is dynamic charge exchange between the channel and independent traps in the gate oxide has been worked out by A. McWhorter [106]. Since then, much work has been developed to the modeling for low-frequency noise in MOSFETs [107-109]. In 1990, K. K. Hung suggested a unified model which combined the carrier number and the mobility fluctuation approaches [110]. In 1992, a more popular form was proposed by G. Ghibaudo with a concept of an input gate voltage noise spectrum [111]. With a general description of G. Ghibaudo [111-113], the fluctuations of drain current stem from the fluctuations of the interface trap charge at the oxide-semiconductor interface. This interfacial oxide trapped charge fluctuation can be regarded as an oxide charge fluctuation δQ_{OX} and it can be equivalent to a fluctuation of the flat band voltage as

$$\delta V_{FB} = \frac{-\delta Q_{OX}}{C_{OX}} \tag{3.14}$$

where C_{OX} is the gate oxide capacitance, W and L the channel width and length, respectively. Considering the relation between the gate voltage and the flat band voltage which is given by

$$V_G = V_{FB} + \phi_S - \frac{Q_i + Q_d + Q_{it}}{C_{OX}} \tag{3.15}$$

where V_G is the gate voltage, V_{FB} the flat band voltage, ϕ_S the surface potential, Q_i the inversion charge, Q_d the depletion charge, and Q_{it} the fast interface state charge. After differentiation of Equation 3.15, the inversion charge fluctuations δQ_i can be obtained by linking the oxide charge fluctuations δQ_{OX}. The relationship is

$$\delta Q_i = \frac{C_i}{C_{OX} + C_d + C_{it} + C_i} \delta Q_{OX} \tag{3.16}$$

where C_d, C_{it}, and C_i is the depletion, fast interface state and inversion charge capacitance, respectively and they are defined as

$$C_d = -\frac{\mathrm{d}Q_d}{\mathrm{d}\psi_S}, C_{it} = -\frac{\mathrm{d}Q_{it}}{\mathrm{d}\psi_S}, \text{and} C_i = -\frac{\mathrm{d}Q_i}{\mathrm{d}\psi_S} \tag{3.17}$$

In Ohmic region, the corresponding drain current fluctuation is derived by differentiating the drain current I_D with respect to the inversion charge

$$\delta I_D = \frac{\mathrm{d}I_D}{\mathrm{d}Q_i}\delta Q_i = \frac{\mathrm{d}I_D}{\mathrm{d}V_G}\frac{\mathrm{d}V_G}{\mathrm{d}\psi_S}\frac{\mathrm{d}\psi_S}{\mathrm{d}Q_i}\delta Q_i \tag{3.18}$$

Using Equation 3.15 and 3.16 incorporating the transconductance g_m (=dI_D/dV_G), the drain current fluctuation becomes

$$\delta I_D = -g_m \delta V_{FB} = g_m \frac{\delta Q_{OX}}{C_{OX}} \tag{3.19}$$

and the normalized drain current spectral density can be obtained as

$$\frac{S_{Id}}{I_D^2} = \frac{g_m^2}{I_D^2}\frac{S_{Qox}}{WLC_{OX}^2} = \frac{g_m^2}{I_D^2} S_{Vfb} \tag{3.20}$$

From Equation 3.20, the normalized drain current noise S_{Id}/I_D^2 of the carrier number fluctuation model is proportional to $(g_m/I_D)^2$ and the curve starts from a plateau at weak inversion before decreasing as I_D^{-2} at strong inversion. Figure 3.4 exhibits the comparison between the carrier number fluctuation (precisely including correlated mobility fluctuations) and Hooge mobility fluctuation model by theoretical calculation [111].

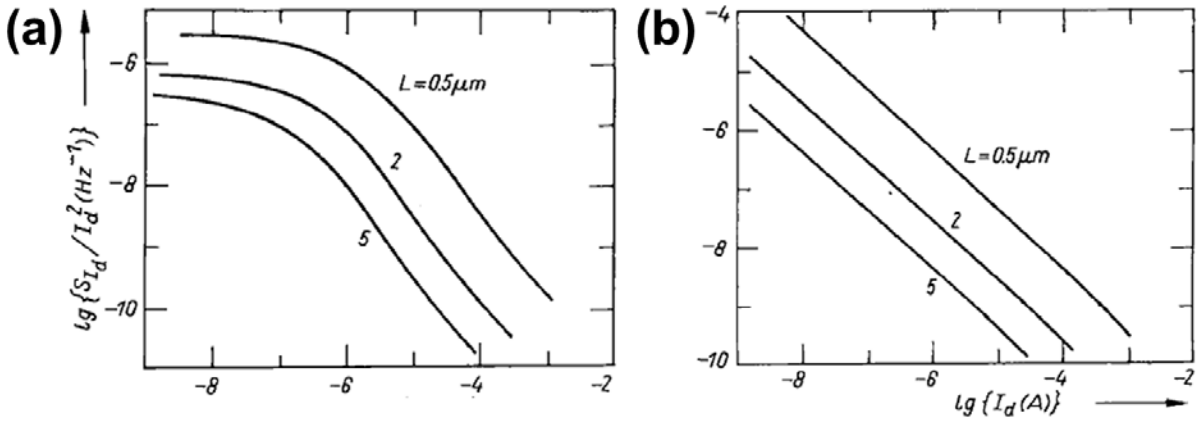


Figure 3.4 Theoretical variations of the normalized drain current power spectral density as given by (a) the carrier number fluctuation model and (b) the Hooge mobility fluctuation model for various channel lengths [111].

3.3.2.1 Tunneling process

As mentioned previously, in the McWhorter carrier number fluctuation model, the fluctuation of current is due to the inversion charge fluctuations at the oxide-semiconductor interface. The salient assumption of this model is the tunneling process which explains the physical trapping mechanisms of charge carriers into the oxide. In the tunneling process, the trapping time constant τ_{tunnel} is given as

$$\tau_{tunnel} = \tau_0(E) \cdot \exp\left(\frac{z}{\lambda}\right) \tag{3.21}$$

where τ_0 is the typical attempt time, taken as 10^{-10} s, z the distance of a trap from the interface (z=0), and λ the tunneling distance. The tunneling distance (or attenuation length) λ can be estimated by the Wentzel-Kramers-Brillouin (WKB) theory and it is defined as [114]

$$\lambda = \left[\frac{4\pi}{h}\sqrt{2m^*\Phi_B}\right]^{-1} \tag{3.22}$$

where Φ_B is the tunneling barrier height seen by the carriers at the interface, h the Planck constant, and m^* the effective mass of the charge carrier. Hence the values of λ are different depending on materials. It has been known as 10^{-8} cm (≈1 Å) for

Table 3.1 Tunneling distance λ calculated for SiO_2, HfO_2 and Al_2O_3 on Si [87].

Dielectric	λ (cm, for electron)	λ (cm, hole)
SiO_2	1×10^{-8}	0.81×10^{-8}
HfO_2	2.1×10^{-8}	
Al_2O_3	1.1×10^{-8}	

Si/SiO_2 system and the λ values for other major dielectrics on the Si system are summarized in Table 3.1. By applying the Equation 3.21, the flat-band voltage spectral density takes the form as

$$S_{Vfb} = \frac{q^2 kT\lambda N_t}{WLC_{OX}^2 f^{\gamma}} \tag{3.23}$$

where f is the frequency, γ the exponent close to 1, k the Boltzmann constant, T the absolute temperature, and N_t is the volumetric oxide trap density (eV/cm^3). For equivalent energy tunneling processes, the traps located within kT from the quasi-Fermi level only activate for the fluctuations [115]. Therefore, the spatial distribution of traps located from the interface determines the exponent γ. If the traps have uniform distribution then γ is a unity. If the trap distribution is not uniform, γ may deviate from one.

3.3.2.2 Thermally activation process

Another proposed mechanism for the charge carrier trapping is a thermally activated trapping process [116]. The trapping probability decreases exponentially with the activation energy E_a. The time constant $\tau_{thermal}$ for thermally activation process is given by

$$\tau_{thermal} = \tau_0 \cdot \exp\left(\frac{E_a}{kT}\right) \tag{3.24}$$

and the flat-band voltage spectral density is [113],

$$S_{Vfb} = \frac{q^2 k^2 T^2 N_{it}}{WLC_{OX}^2 f^{\gamma} \Delta E_a} \tag{3.25}$$

where ΔE_a is the amplitude of the activation energy dispersion and N_{it} is the oxide trap surface state density (eV/cm^2). The uniform trap distributions of E_a lead to the $1/f$ noise. If the trap density increases with E_a, γ becomes larger than 1 [117].

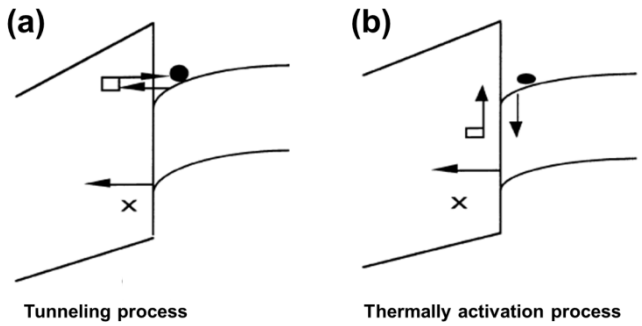


Figure 3.5 Schematic diagrams of (a) tunneling and (b) thermally activation process for the physical trapping mechanism [117].

In Figure 3.5, the schematic diagrams between two different mechanisms are shown. In general, the tunneling process well supports the experimental results but the thermally activation process is also considered for the complete description

of the number fluctuation model.

3.3.3 Carrier number fluctuation with correlated mobility fluctuation model

In the previous section 3.3.2, the carrier number fluctuation model only considers that the drain current fluctuations are caused by the carrier trapping at the interface which induces the variation of carrier number in the channel. However, in a more detailed approach, the influence on the conduction through the Coulomb interaction of the trapped charge carriers should be considered because the trapped charge carriers can lead to the mobility scattering of charge carriers. Thus, the mobility scattering induces additional drain current fluctuations due to the oxide charge fluctuations. With this idea, the drain current fluctuations can be expressed as [111]

$$\delta I_D = \delta V_{FB} \left.\frac{\partial I_D}{\partial V_{FB}}\right|_{\mu_{eff}=const} + \delta\mu_{eff} \left.\frac{\partial I_D}{\partial \mu_{eff}}\right|_{V_{FB}=const} \tag{3.26}$$

Assuming the general mobility law, $1/\mu_{eff} = \alpha_C Q_{OX} + 1/\mu_0$ where α_C is the Coulomb scattering coefficient and it allows to obtain the drain current fluctuations as

$$\delta I_D = -g_m \delta V_{FB} \mp \alpha_C I_D \mu_{eff} \delta Q_{OX} \tag{3.27}$$

where the negative and positive signs of the second term are used for acceptor-like traps and donor-like traps, respectively [110]. The Coulomb scattering coefficient α_C are reported to be about 10^4 and~10^5 Vs/C for n- and p-type conventional MOSFETs, respectively. Based on Equation 3.27, the normalized drain current S_{Id}/I_D^2 and equivalent input gate voltage spectral density S_{Vg} can be derived as

$$\frac{S_{Id}}{I_D^2} = \left(1 \pm \alpha_C \mu_{eff} C_{OX} \frac{I_D}{g_m}\right)^2 \frac{g_m^2}{I_D^2} S_{Vfb} \tag{3.28}$$

and

$$S_{Vg} = \left(1 \pm \alpha_C \mu_{eff} C_{OX} \frac{I_D}{g_m}\right)^2 S_{Vfb} \tag{3.29}$$

In Equation 3.28, the first term in the parentheses is for the carrier number fluctuations in the channel and the second term indicates the correlated mobility fluctuations by trapped charge at the interface. If the α_C is zero and S_{Vg} is same to S_{Vfb}, it means that the mobility is independent of interface charge. On the contrary, if the α_C is high enough (typically $\alpha_C \geq 10^4$

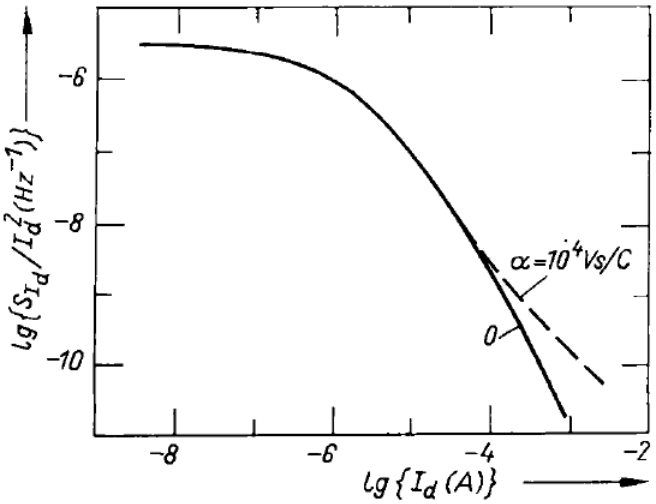


Figure 3.6 Theoretical variations of the normalized drain current noise spectrum with drain current as given by the carrier number fluctuation model with (α_C=10^4 Vs/C) and without (α_C=0 Vs/C) correlated mobility fluctuations [111].

Vs/C for electrons), the slope of S_{Id}/I_D^2 at the high gate voltage is changed as shown in Figure 3.6. It is due to the influence of correlated mobility scattering at strong inversion. For *n*-type MOSFETs, the values of $\alpha_{C,\ n\text{-type}}$ are around 1×10^4 Vs/C while *p*-type MOSFETs have much larger values of $3\sim20\times10^4$ Vs/C [87]. However, the impact of correlated mobility fluctuations makes a small correction and it is still based on the carrier number fluctuation model.

3.4 Noise measurement system configuration

To characterize low-frequency noise, a well-configured measurement system is essential because the noise measurement is sensitive and delicate process. The system configuration consists of several electronic parts; a power (voltage or current) source, a pre-amplifier, a spectrum analyzer, and supplementary parts like a frequency filter to cut unessential external noise. A schematic of noise measurement system configuration is illustrated in Figure 3.7. In principle, the noise signal can be obtained by converting from the output signal (current or voltage) in time domain to the power spectral density in frequency domain through Fourier transform method.

For the operation of semiconductor device, the power source is generally recommended in the form of a voltage or a current source only having DC signal. However, the conventional power source operated with AC power supply has additional AC signal at either 50 or 60 Hz because most electric power is generated at 50 or 60 Hz. Such signals can be easily exposed the noise measurement in the shape of a peak near 50 or 60 Hz. This kind of noise may not be crucial depending on the situations. Nevertheless, in general, batteries which have no AC

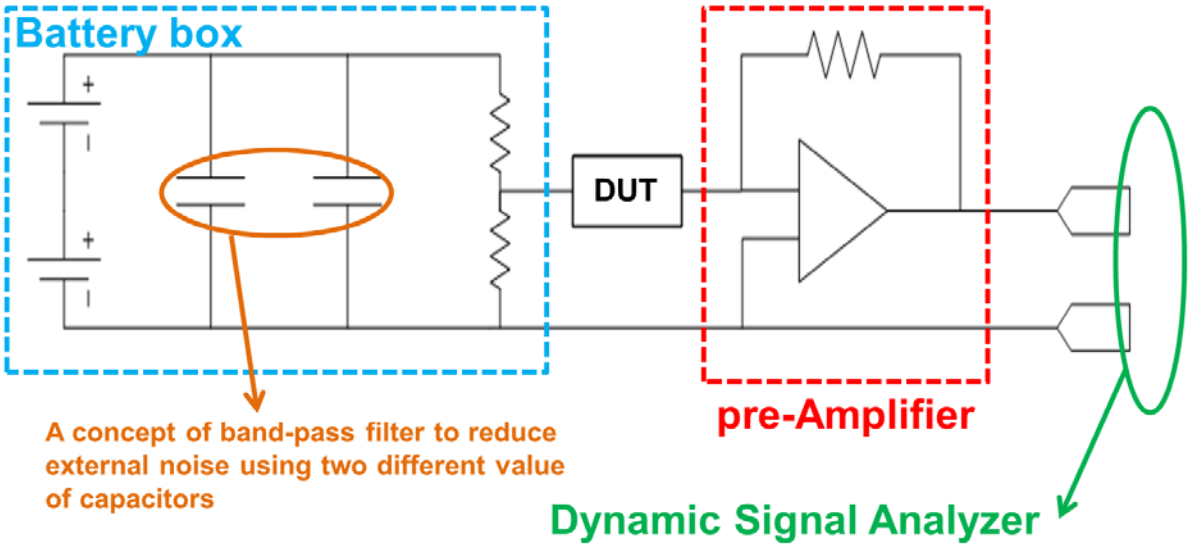


Figure 3.7 Schematic diagram of low-frequency noise measurement system.

signals are used to obtain more clear data. Indeed, the level of noise signal in devices is quite small compared to the output signal (i.e. current) so that there is a need to enlarge the noise signal for the data acquisition. Therefore, the pre-amplifier is an essential part for the noise measurement and the current-voltage pre-amplifier has been well used since the input signal of conventional spectrum analyzer is a voltage signal in contrast to a current signal which is interesting for us. For the noise measurement, the pre-amplifier is required to have low noise, high gain and bandwidth. Figure 3.8 (a) shows an example of low-noise current pre-amplifier (SR570, Stanford Research System) which is used in these study.

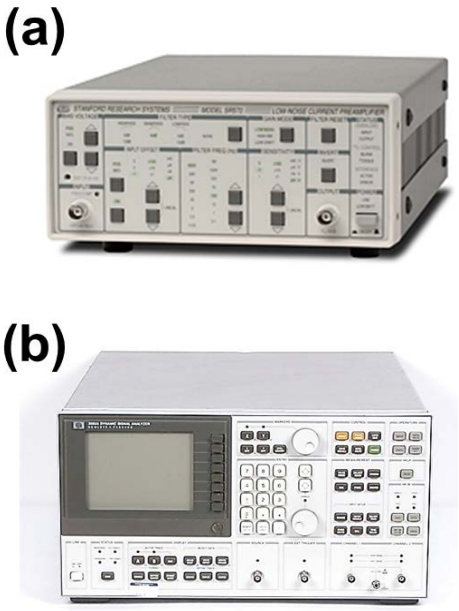


Figure 3.8 Noise measurement system: (a) a pre-amplifier (SR570, Stanford Research System) and (b) a dynamic signal analyzer (HP3562, Agilent).

When the noise signal is sufficiently amplified, the last part is performed by a spectrum analyzer enabling to convert the discrete signal in the time domain to the frequency domain using the Fast Fourier Transform. The conventional quantity for the noise analysis, the power spectral density, can be usually obtained with the spectrum analyzer as shown in Figure 3.8 (b). In recent, along with the development of computer engineering, these conversion works with the Fourier transform can be proposed with a computer system with appropriate hardware and software. For example, the data in time

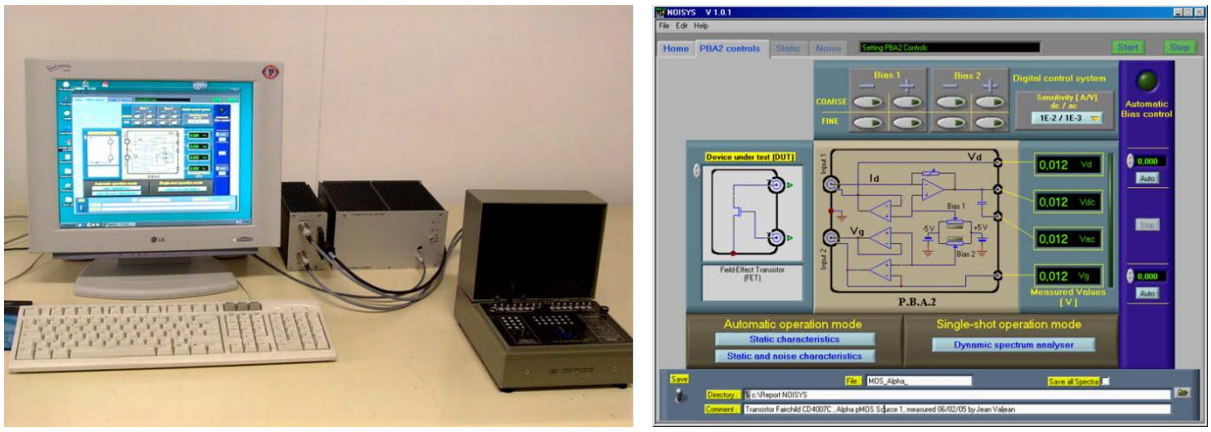


Figure 3.9 Computer based noise system: 3PNMS at IMEP-LAHC (Synergie-concept).

domain from the pre-amplifier can be directly collected into the computer through the DAQ product and converted into the frequency domain with proper software providing Fourier transform method. In this thesis, the noise measurements were performed with either a classical system with several equipment and a computer based system called the Programmable Point Probe Noise Measuring System (3PNMS, Synergie-concept). The 3PNMS located at IMEP-LAHC is an efficient automation system for the noise measurement (Figure 3.9) [118].

After the configuration of noise system, an important work is the suppression of background noise of both inside and outside the system for the accurate measurement. The system should effectively remove any external noises coming from the environment such as light, sound, vibration, and any other sources which can affect the measurement. If such external noises cannot be sufficiently removed or reduced during the noise measurement, inaccurate noise data will be obtained. Thus, the appropriate shielding techniques are important. A typical shielding method consists in isolating the sample and equipment from outside with a grounded metal box. With applying the enclosure, shielded cables are also important. Despite of the effective isolation of the sample and equipment, the noise can be existed due to an unexpected electric shock. Therefore, all equipment involving the enclosure, cables, and any other parts should be grounded. At this time, it should be noted not to make a ground loop which refers to an unwanted signal in a conductor connecting two points due to the potential differences even if they are supposed to be at the same potential. It has been known that the ground loops created by improperly designed and installed equipment are a major source of noise and interference [119]. To avoid the ground loop, it is important to make a single-ended ground. In Figure 3.10, the schematic diagrams involving the ground

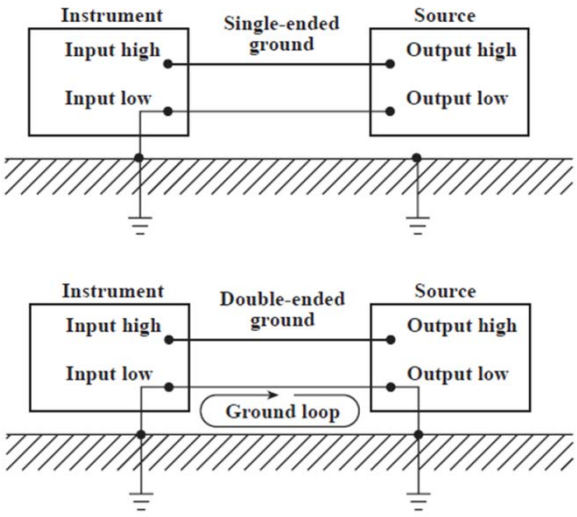


Figure 3.10 Differences between single- and double-ended ground systems to avoid the ground loop [120].

loop of single- and double-ended ground configuration are shown [120].

If the noise from outside is properly suppressed with appropriate shielding and grounding techniques, the noise in the system (i.e. a system noise) has to examined and reduced since the system noise determines a limit of determination in the noise measurement system. The system noise is mainly determined by the pre-amplifier even though the pre-amplifier operates with batteries too. For this reason, a low-noise pre-amplifier is generally used and the noise level of pre-amplifier is also confirmed to the system limitation. The recommended system noise level in current power spectrum unit is below ~ 10^{-26} A^2/Hz. The minimum noise level of 3PNMS and SR570 pre-amplifier are measured about 1.69×10^{-27} A^2/Hz and 2×10^{-29} A^2/Hz, respectively. Moreover, it has to be examined with different sensitivity in the amplifier system since the system noise can be changed with the different sensitivity.

3.5 Summary

In this chapter, in semiconductor devices, the theoretical background of electronic noise such as thermal, generation-recombination, random telegraph signal noise, and 1/*f* noise were reviewed involving their physical meanings. Especially, we focused on the study of low-frequency noise. Among of them, 1/*f* noise as a universal type of noise is well observed in various materials and device structures. To understand the origin of low-frequency noise in MOS structures, herein we introduced two representative models: one is the Hooge mobility fluctuation model and the other is the carrier number fluctuation model which is also considered the correlated mobility fluctuations by the trapped charges at the interface. The origin of fluctuations is originated from the carrier types, device structures, interface traps, defects, and etc. Finally, the system configuration was presented to obtain the low-frequency noise in semiconductor devices. It was noted that the shielding and grounding are essentially required to preventing disturbance by external noise and the system noise coming from the

equipment (e.g. low-noise amplifier) is also important.

Experimental Results

Chapter 4 Multi-Gate MOSFETs

Chapter 5 Nanowires and Nanotubes

Chapter 6 Graphene

Chapter 4 Multi-Gate MOSFET

4.1 Background: From planar to 3-D structure

A state-of-the-art planar MOS transistor is the representative device structure for CMOS technology based on bulk silicon and it has been in continuous efforts to decrease the device size and better electrostatic control. As decreasing the channel length, there are three main limiting factors which are the gate leakage, the source-drain leakage, and the junction capacitance [121]. The gate leakage is coming from the reduced thickness of silicon dioxide (SiO_2) and the concept of equivalent oxide thickness (EOT) has been used for the comparison of various films and thickness. EOT is given by

$$EOT = \frac{k_{SiO2} \times t_x}{k_x} \tag{4.1}$$

where k_{SiO2} is the dielectric constant of SiO_2 (i.e. k_{SiO2} = 3.9), t_x and k_x the thickness and the dielectric constant for the film of interest, respectively. Since about 3 ~ 4 nm of oxide thickness is known to be a leakage current limit of SiO_2, high-k materials are using for sub-nm scale transistors. And there are several effects for the source-drain leakage, which are named short-channel effects implying less control of the channel region by the gate [5]. To reduce short-channel effects, the device structure was improved from a bulk to a fully-

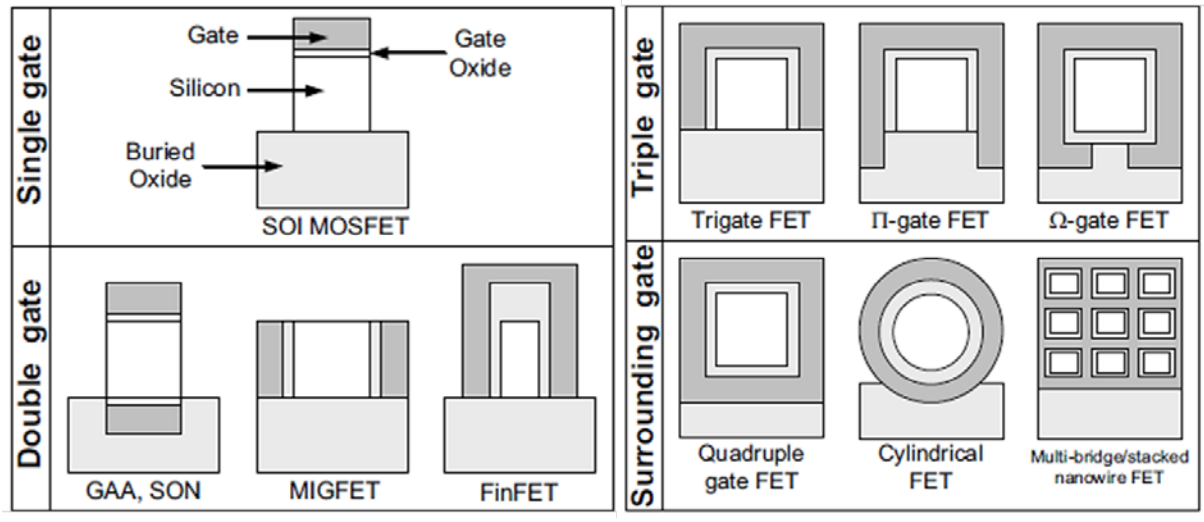


Figure 4.1 Different gate configurations [5].

depleted SOI (FD-SOI) having the buried oxide [122]. Nevertheless, the inconvenience of increased junction capacitance and body effect demands more efficient device configuration enabling various types of multi-gate structure as shown in Figure 4.1 [123]. The DG-MOSFET by sandwiching a fully depleted SOI device between two gate electrodes was proposed by T. Sekigawa and Y. Hayashi in 1984 [124]. In 1990, D. Hisamoto presented a new structure named 'fully DEpleted Lean-channel TrAnsistor (DELTA)' [125]. The DELTA structure is a basis for the current FinFET structure. Gradually, the multi-gate FETs spreads to Π-gate, Ω-gate, and GAA FETs [28], [126], [127].

4.2 FinFETs

In the section 4.2, the electrical transport and low-frequency noise characteristics in high-*k*/metal-gate FinFETs, which are one of the famous multi-gate structures, were investigated with different channel width and length. The FinFET architecture has been proposed as a solution to overcome the short-channel effects together with several benefits such as steep subthreshold slope, low body coefficient, and high switching speed [128]. In this study, the FinFETs fabricated with standard silicon on insulator (SOI) process at IMEC (Leuven, Belgium) were used [129].

4.2.1 Device structure

A detailed fabrication process is as follows: the top silicon layer on SOI wafer was thinned down to 65 nm of thickness (T_{Si}) and it was non-intentional by doped with background Boron doping of 10^{15} cm^{-3}. The silicon layer was etched having multi-gate structures for the channel and the un-doped channel region results in less mobility degradation by reducing the impurity scatterings in the channel. For the gate oxide, HfSiO was deposited having 1.7 nm of equivalent oxide thickness by MOCVD process. A 5 nm of TiN, capped with 100 nm poly-Si, was used for the gate electrode. The source/drain (S/D) region for metallization was heavily doped with 2×10^{20} cm^{-3}. Figure 4.2 (a) shows transmission electron microscope (TEM) images of a FinFET having HfO_2 gate dielectric and TiN metal-gate from IMEC. The gate configuration is close to Ω-gate structure.

3-D Schematic view and longitudinal cross section exhibiting the doping profiles of the FinFET was illustrated in Figure 4.2 (b) and (c), respectively. From Figure 4.2 (c), the device

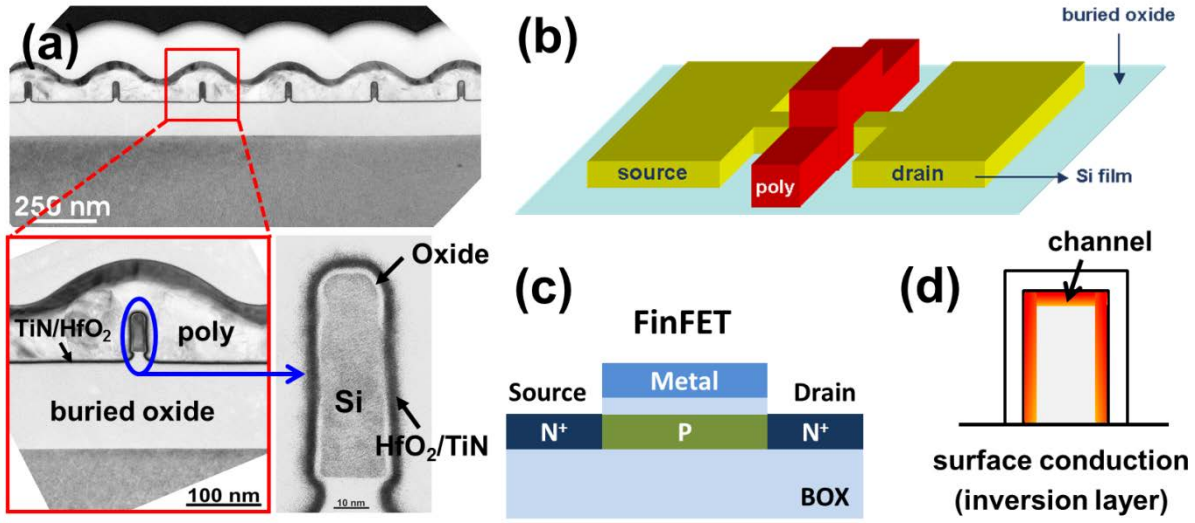


Figure 4.2 (a) Transmission electron microscope (TEM) images of high-k/metal-gate FinFET. (The images were obtained from IMEC for the TEM image request of our devices. Both device structures are similar.) (b) 3-D Schematic view of a FinFET (c) Longitudinal cross section showing the doping profiles in the inversion-mode FinFET (d) Electron concentration profile in the inversion-mode FinFET having surface conduction.

structure is the same to the conventional enhancement-mode transistor with p-doped body region for channel inversion and heavily n-doped S/D region [130]. For the inversion-mode FinFET, the conduction will be occurred along the top surface and two sidewalls when the device is turn on (Figure 4.2 (d)). Therefore, it might be recalled that a FinFET has the surface conduction. The surface conduction in FinFETs also causes some issues [131-134]. For example, an early current saturation at high gate voltage can be observed in the FinFET and it is known to be due to the mobility degradation by the surface roughness scattering [132].

4.2.2 Electrical characterization at the fin width variation

4.2.2.1 DC characteristics

The electrical measurements of FinFETs were performed at room temperature with the programmable point probe noise measurement system (3PNMS, Synergie-concept) that is enabling to measure the static and noise characteristics at the same time. The drain voltage is fixed at 10 mV to prevent the device deterioration. To observe the width dependence, the fin width (W_{Fin}) is varied with 10, 20, 40, 65, 130, 250, 500, and 1000 nm. The fin height is

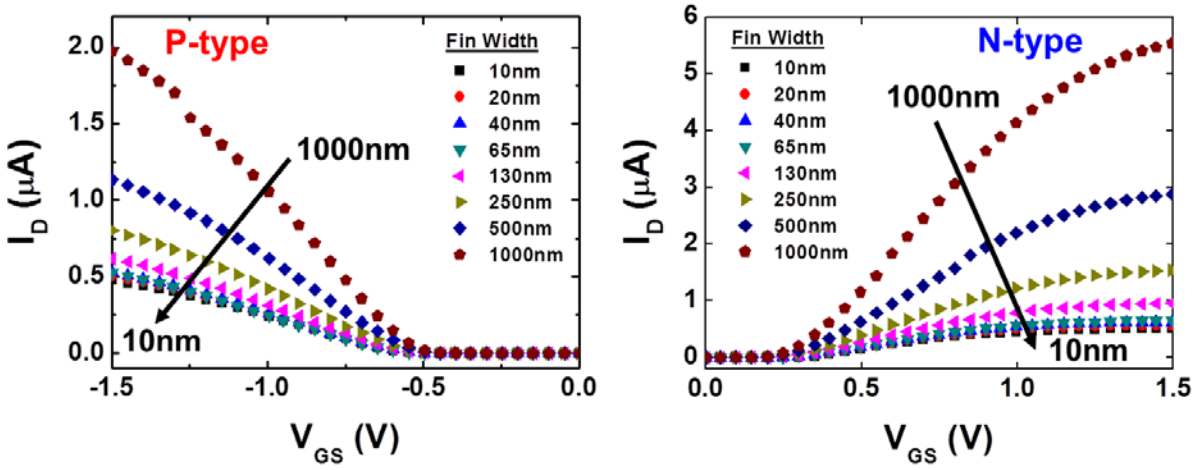


Figure 4.3 I_D-V_{GS} characteristics for *n*- and *p*-type FinFETs at V_{DS}=10 mV. The channel length is 1 μm and the fin width was defined as 10, 20, 40, 65, 130, 250, 500, and 1000 nm.

assumed to be 65 nm for all devices and the channel length is fixed at 1 μm that is long enough to be negligible for the influence of series resistance. For the narrow W_{Fin} of 10, 20, and 40 nm, each device has only one fin structure whereas the others have five number of fin structures. Therefore, the five number of fin structured devices were normalized by the fin number for the correct analysis. In Figure 4.3, typical I_D-V_{GS} characteristics are shown for the *n*- and *p*-type FinFETs with different W_{Fin}. They present a good current behavior versus width variation. The drain current (I_D) of *n*-type devices is approximately three times larger than *p*-type ones because the electron mobility in silicon is larger than hole mobility due to the lower effective mass for electrons [135], [136]. The threshold voltage (V_{TH}) and effective mobility (μ_{eff}) for all devices are compared as shown in Figure 4.4. The V_{TH} is extracted by the second derivative method (Section 2.2.2) and they are in the range of -0.5 ~ -0.55 V and 0.25 ~ 0.3 V

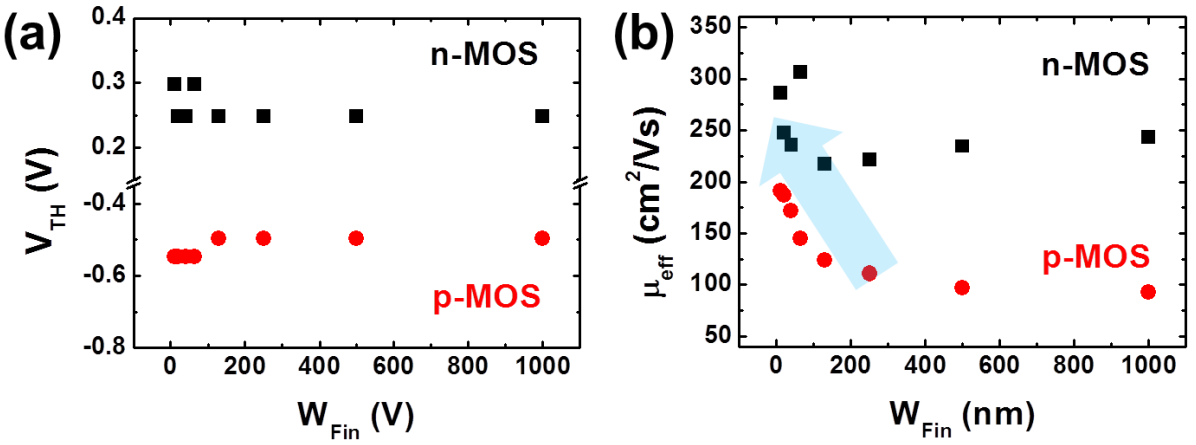


Figure 4.4 (a) Extracted threshold voltages V_{TH} and (b) effective mobility μ_{eff} for *n*- and *p*-type FinFETs as changing W_{Fin}. No V_{TH} shift could be observed and μ_{eff} slightly increased as decreasing W_{Fin}.

for the *p*-type and *n*-type devices, respectively (Figure 4.4 (a)). There is no significant V_{TH} shift as decreasing W_{Fin} although V_{TH} is slightly increased at narrow W_{Fin}. Likewise, the μ_{eff} is also extracted from Equation 2.20 and they are shown in Figure 4.4 (b). In Figure 4.4 (b), an apparent increase of μ_{eff} is observed for *p*-type devices as reducing W_{Fin} but *n*-type devices show less clear variation. It has been known that the mobility is limited by the sidewall effect because of the surface conduction [137].

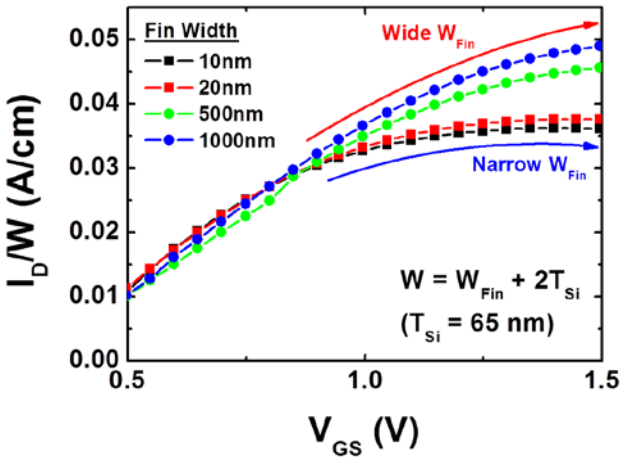


Figure 4.5 I_D normalized by the total channel width (W=W_{Fin}+2T_{Si}) for the narrow and wide channel.

In practice, the sidewall effect is a well-known issue for manufacturing the fin structure. For the fin patterning, reactive ion etching process is generally used but it makes large surface roughness at the sidewalls with some damages while the top surface is protected by the mask. In other words, the current at the sidewalls is limited by the surface roughness scattering compared to the top surface. Thus, as decreasing W_{Fin}, the current ratio at the sidewalls is increased in contrast with the reduction of the top surface current. Such current suppression was simply comfirmed by normalizing the current with the total width W_{total} (=W_{Fin}+2T_{Si}) as shown in Figure 4.5. The normalized current of the narrow channel devices are strongly suppressed at the high gate voltage compared to the wide channel devices. Recently, J. W. Lee et al. quantitatively revealed that the mobility in the FinFET structure is limited by the surface roughness at the sidewall using the temperature dependent analysis of effective mobility [128]. They found that the surface roughness scattering at the sidewalls is three times stronger than at the top surface for *n*-type FinFETs while it is smaller for *p*-type ones.

4.2.2.2 LF noise characteristics

For the low-frequency (LF) noise analysis, the drain current noise power spectrum (S_{Id}) was measured as changing V_{GS} for each different W_{Fin} at the frequency from 10 Hz to 10 kHz. For the FinFET at W_{Fin}=10 nm, the power spectra as a function of the frequency are plotted for the different V_{GS} as shown in Figure 4.6. They are in the combination of Lorentzian and

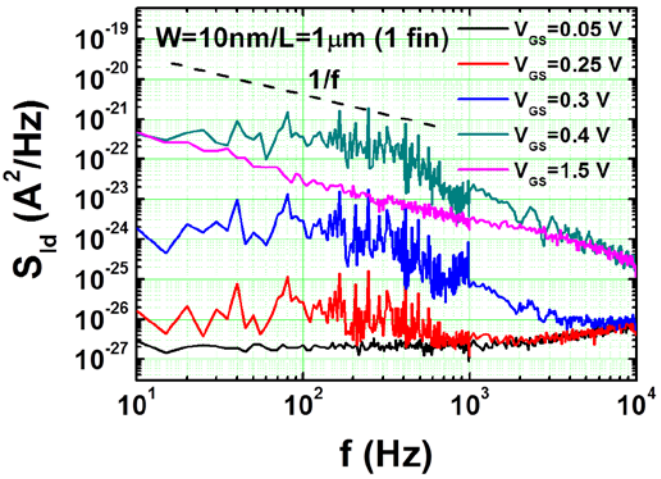


Figure 4.6 Drain current noise power spectra (S_{Id}) as a function of the frequency for the 10 nm fin width FinFET with different gate voltages (V_{GS}).

1/*f* behaviors. At the V_{GS} < ~1.2 V, S_{Id} is close to Lorentzian behavior which is in the shape of generation-recombination (g-r) or random telegraph signal (RTS) noise but it changed to 1/*f* noise at higher V_{GS}. It might show that the carrier number fluctuation (CNF) for 1/*f* noise comes from the superposition of RTS noise with different trap level. The tendencies are similar for all devices apart from the fin width and polarity of carrier.

To understand the LF noise origin of FinFETs, the S_{Id} was normalized by I_D^2. If the noise origin is carrier number fluctuations, S_{Id}/I_D^2 will be proportional to $(g_m/I_D)^2$ whereas it will decrease as following the inverse drain current for the Hooge mobility fluctuation (HMF) model. Furthermore, the total channel widths for the analysis were considered by multiplying the S_{Id}/I_D^2 and dividing for I_D since the noise and current depend on the channel width. Figure 4.7 exhibits the normalized noise spectral densities with each different fin width for *n*-type and *p*-type FinFETs. For both devices, a near plateau curve is appeared below threshold and it dramatically decreases as increasing the current that is inversely proportional to I_D^2. These results show that the origin of LF noise in FinFETs is due to number fluctuations at oxide-

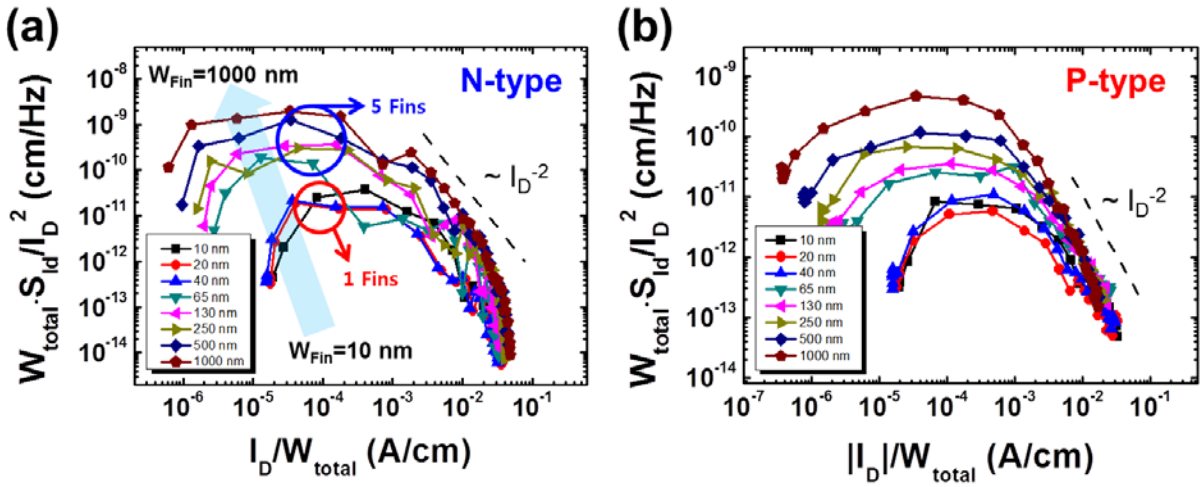


Figure 4.7 Normalized current noise spectral densities with the drain current and total channel width (W_{total}=W_{Fin}+2·T_{Si}) as a function of the total channel width normalized drain current for *n*- and *p*-type FinFETs.

semiconductor interface regardless of device type.

As mentioned in previous chapter, the influence of surface roughness of sidewalls in the FinFET structure is important as decreasing the fin width. Similarly, the surface roughness also can affect the interface quality related to the trap density. In the previous work, K. Bennamane et al. studied that the impact of the top surface and sidewalls on the LF noise in FinFET structures by the separated extraction technique [138]. Here, with this technique, the variations of S_{Id} with different W_{Fin} are plotted to separate the top surface and side-wall of drain current noise contribution as shown in Figure 4.8. However, the linearity of extracted S_{Id} is not good unlike the K. Bennamane's work and it is still not enough to fit after data smoothing. It is thought that the extraction technique is not good for the noise analysis because the noise data is rather sensitive compared to typical *I-V* measurement.

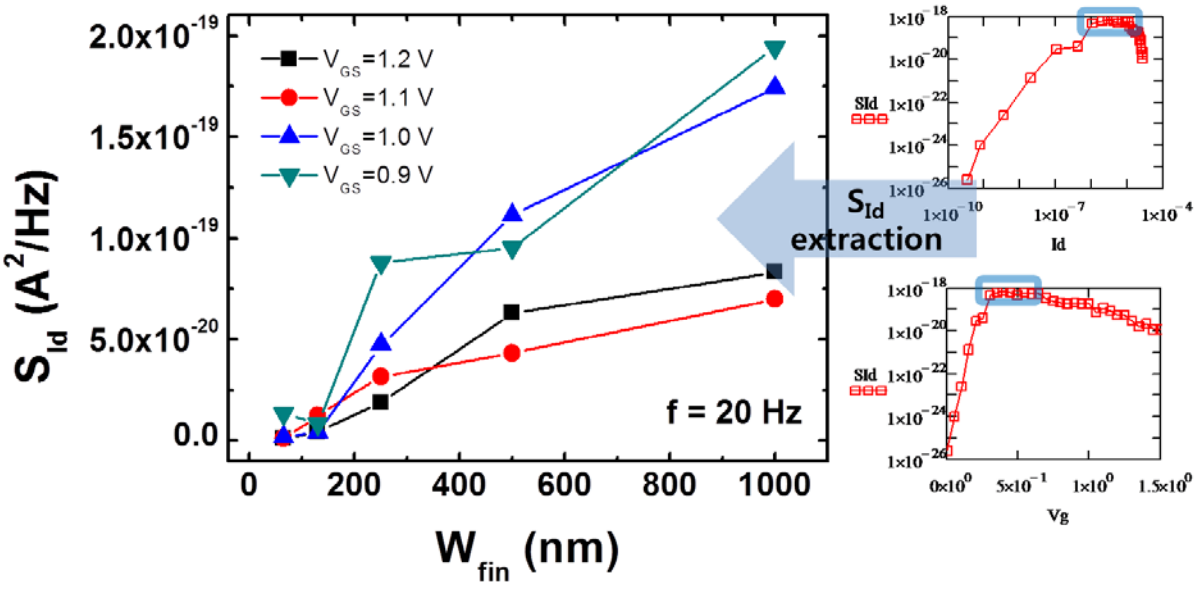


Figure 4.8 Drain current noise was plotted as changing the fin width to separate the influence of the top surface and side-wall in the FinFET.

Instead the trap extraction for each surface, by the CNF model, the volume trap density N_t can be estimated from the input-referred noise spectral density S_{Vg} at flat band, i.e. S_{Vfb} is given by

$$N_t = \frac{W_{total} L_G C_{OX}^2 f}{q^2 kT\lambda} S_{Vfb} \tag{4.2}$$

where S_{Vfb} is the flat band voltage noise defined as $c\cdot(S_{Id}/I_D^2)\cdot(I_D/g_m)^2$ and λ is the tunneling attenuation length in Equation 3.22. For the SiO_2/Si system, λ is about 1×10^{-8} cm but it varies depending on the system. However, we could not find proper λ value for the HfSiO/Si system

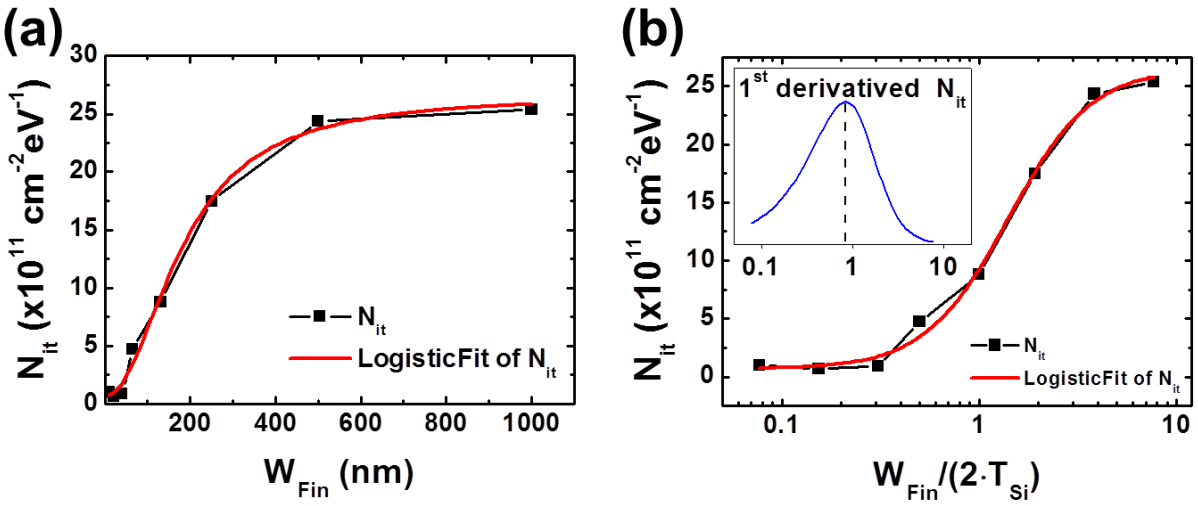


Figure 4.9 Interface trap densities (N_{it}) as a function of (a) W_{Fin} and (b) normalized W_{Fin} by the fin height (T_{Si}). A red solid line is a fitting curve by the logistic function. The inset of (b) is the first derivation the N_{it} – $W_{Fin}/2{\cdot}T_{Si}$ characteristic.

so that the interface trap density N_{it} ($=\lambda \times N_t$) is used for the comparison. Considering different fin number for each device, N_{it} was extracted with different W_{Fin}. As shown in Figure 4.9 (a), extracted N_{it} for the *n*-type FinFET is varied with different fin width. For the wide channel width, they are in the range of 2×10^{12} $cm^{-2}eV^{-1}$ and it decreases as reducing W_{Fin} finally saturates about 1×10^{11} $cm^{-2}eV^{-1}$ at the narrow channel width. A solid red line is a fitting line by the software. A logistic dose-response function is used and can be expressed as

$$f(X) = \frac{A_1 - A_2}{1 + (X / X_0)^p} + A_2 \tag{4.3}$$

where A_1 and A_2 are the initial and final value of N_{it}, X_0 is the standard value for the variation of N_{it}, and p is the exponent. After the fitting process, the extracted parameters are as follows: A_1=6.7×10^{10}, A_2=2.5×10^{12}, X_0=182, and p=2. There are similar to minimum and maximum values of N_{it}. To observe the influence between top surface and sidewalls, W_{Fin} is normalized with $2T_{Si}$ as shown in Figure 4.9 (b). The inset indicates the maximum point of N_{it} variation rate which is at W_{Fin}=$2T_{Si}$=130 nm.

For *p*-type FinFETs, N_{it} was also extracted and such N_{it} variation was also observed in *p*-type devices as shown in Figure 4.10 (a). It looks that N_{it} in the *p*-type devices are slightly larger than in the *n*-type ones but it is noted that the tunneling distances for electrons and holes are different. Since the tunneling distance for electrons is longer than for holes, the volume trap density for both devices might be similar. Together with N_{it} extraction, the Coulomb scattering coefficients (α_C) by the carrier number fluctuation with correlated

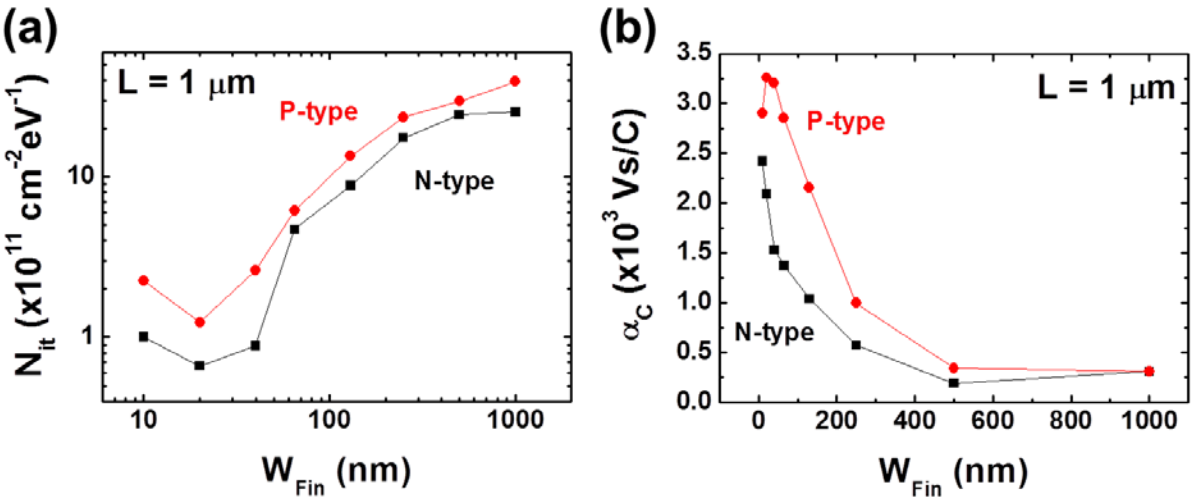


Figure 4.10 (a) Log (N_{it}) vs Log (W_{Fin}) and (b) Coulomb scattering coefficient α_C by the CNF+CMF model for *n*- and *p*-type FinFETs.

mobility fluctuation (CNF+CMF) model are compared in Figure 4.10 (b) and there is no significant α_C which are in the range of 10^3 Vs/C. However, α_C is increased as decreasing W_{Fin}. It might be due to the influence of trapped charge at the sidewalls.

4.2.3 Electrical characterization of the length dependence

4.2.3.1 DC characteristics

The channel length dependence was also observed for the *n*-type FinFETs. For the channel structure, there are five numbers of fins which have W_{Fin}=130 nm and their pitch size (the

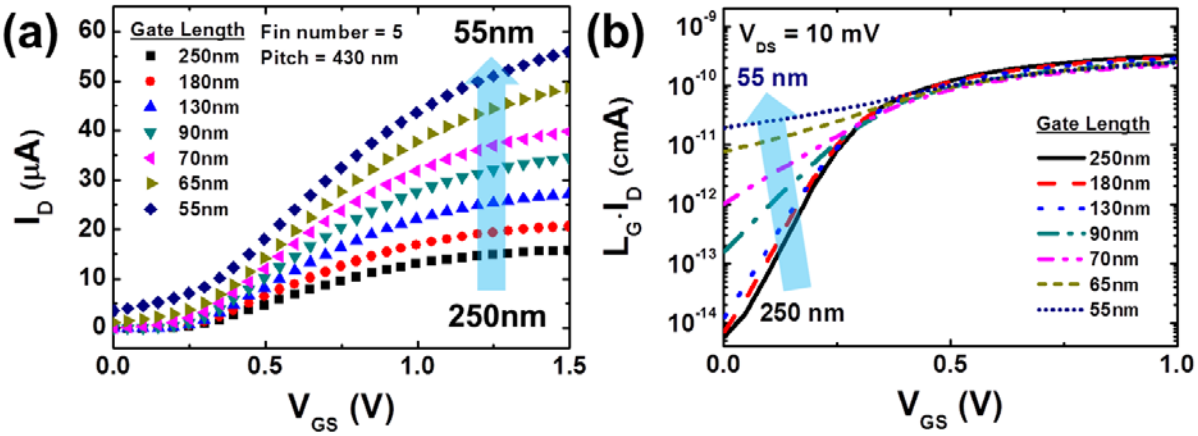


Figure 4.11 (a) I_D-V_{GS} characteristics of FinFETs with different channel lengths at V_{DS}=10 mV. The FinFETs have 5 fins and the pitch size is about 430 nm. (b) Normalized I_D with L_G is plotted in log scale and the dramatic increase of off-current as decreasing L_G is observed.

distance from left side of first fin to next left side of second fin) is about 430 nm. The I_D-V_{GS} characteristics are shown in Figure 4.11 (a). As decreasing the gate channel length (L_G), the current is increased together with growth of off-current at subthreshold (i.e. subthreshold leakage current). For clear understanding of the off-current transition, the drain current was normalized with L_G and it was shown in log scale (Figure 4.11 (b)). The on-current above the threshold showed almost same level of drain current but the off-current was significantly increased when L_G is reduced. Especially, below 100 nm gate cannel length, the off-current is drastically increased. It is one of the short-channel effects by weak electrostatic control of the gate electrode as decreasing L_G.

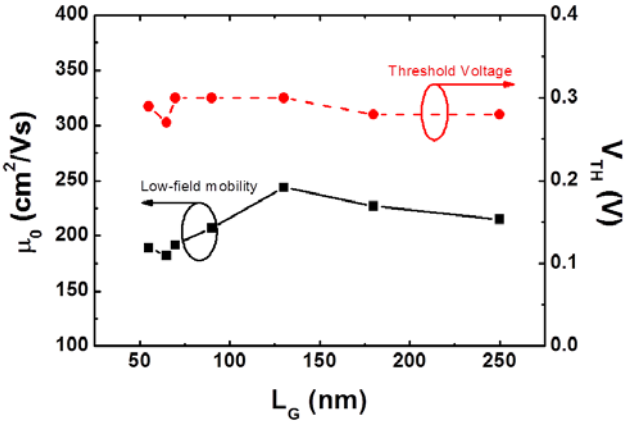


Figure 4.12 Extracted threshold voltage and low-field mobility by Y-function method.

The extracted threshold voltage (V_{TH}) by the second derivative method is about 0.25 V and the low-field mobility (μ_0) by the simple effective mobility calculation (Equation 2.20) is suppressed from 188 to 146 cm^2/Vs as decreasing the channel length. However, in the short-channel, the influence of series resistance cannot be negligible so that the V_{TH} and μ_0 were also calculated with the Y-function method which can reduce the parasitic series resistance effect. Figure 4.12 exhibits the variation of V_{TH} and μ_0 as changing L_G. They are roughly ~ 0.3 V and ~ 200 cm^2/Vs for V_{TH} and μ_0, respectively apart from the different L_G.

4.2.3.2 LF noise characteristics

For *n*-type FinFETs with channel length variation, LF noise is observed in the same manner as for the channel width dependence. In Figure 4.13 (a), the drain current noise spectrum is normalized with the drain current and the channel length. Their behaviors are well explained with the CNF model. Similarly, the interface trap densities for the channel length dependence were also extracted and they plotted in Figure 4.13 (b). The N_{it} is in the range of roughly 10^{10} ~ 10^{11} cm^{-2}eV^{-1} which is similar or rather smaller than long channel device (L_G=1 μm, 8.8×10^{11} cm^{-2}eV^{-1}) and the behavior is that N_{it} is decreased linearly until 70 nm channel length, but it arises again. It is interesting behavior which might be due to the

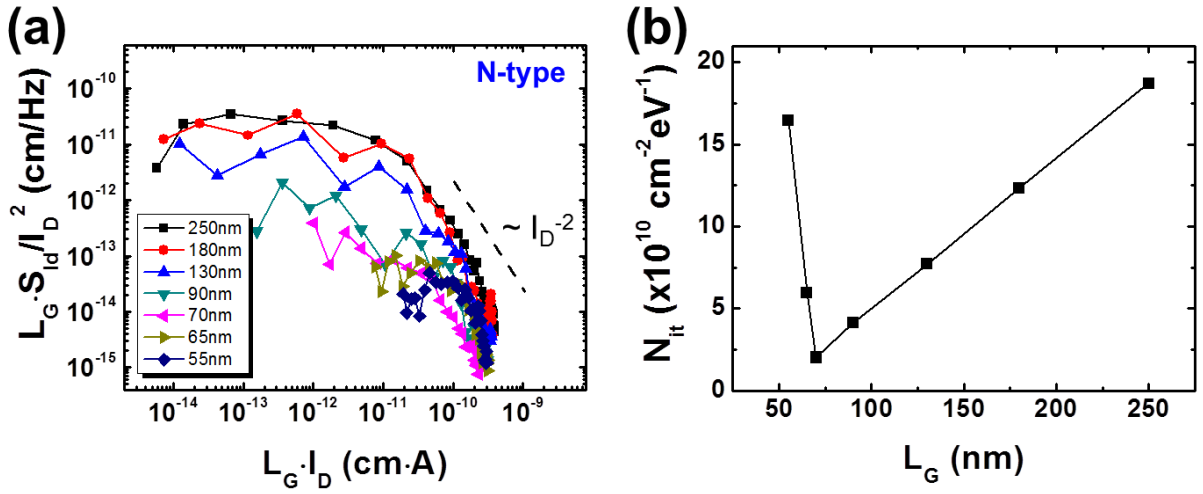


Figure 4.13 (a) Normalized current noise spectral densities with the drain current and channel length as a function of the channel length normalized drain current for *n*-type FinFETs. The channel length is varied from 250 nm to 55 nm. (b) Extracted interface trap density for each channel length.

influence of impurities near the source and drain. However, it is not studied in detail with additional analysis and measurement yet.

4.2.4 Device simulation for the fin width dependence

4.2.4.1 Basic concept of simulation

In recent, as fabrication processes and devices become more complex, it is also becoming more complex to understanding the device and process behaviors. For the understanding the device properties such as electrical, optical, and thermal behaviors, doing the experiments is a best solution obviously but it supplementally demands much higher costs for the experiments with number of possible variations. For this reason, a simulation work has been widely used for predicting and understanding the device properties. There are two kinds of simulation methods. If we can find appropriate mathematical models for the device properties, we can easily obtain the results after the mathematical calculation. It is an analytic method. However, the device structure becomes

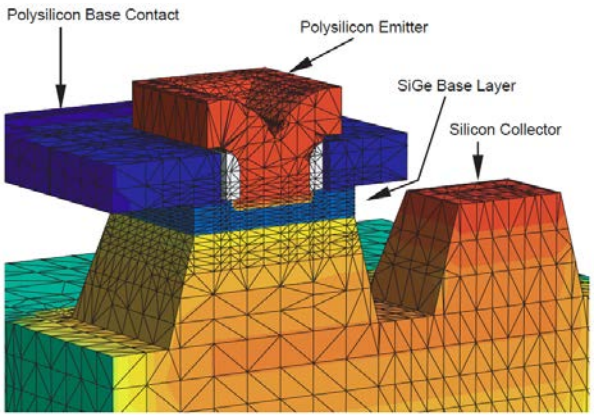


Figure 4.14 Simulation example of 3-D SiGe HBT structure (Synopsis).

more complex so that it is getting difficult to find the proper expressions for the devices. In this case, the analytic method is impossible. In contrast, a numerical method is a more useful and popular technique for the simulation of complex devices and depends on the computing power generally. It is based on calculating properties at a number of points or nodes in the device region by splitting the small spaces as shown in Figure 4.14. The device simulation can provide information the device properties in both steady state and during transient conditions. In general, the models are based on the solution of Poisson's equation and continuity equations.

In this section, we did the device simulation for the FinFET structure with the channel width variation by a FlexPDE (PDE Solution Inc.). The FlexPDE is a general-purpose tool for obtaining numerical solutions based on the finite element method [139]. The finite element method is a numerical technique for finding solutions of partial differential equations [140].

4.2.4.2 Results of 2-D simulation

The simulation results for the conductance variation and the LF noise of FinFETs with fin width variation were obtained by solving Poisson equation across a two-dimensional section of the structure and coupling it to the drift-diffusion equation. The device parameters such as channel doping concentration, low-field mobility, and volume trap density are used based on the experimental parameters of a certain device. In same conditions, the simulations were performed as changing the fin width. Figure 4.15 exhibits the simulation results of I_D-V_{GS}

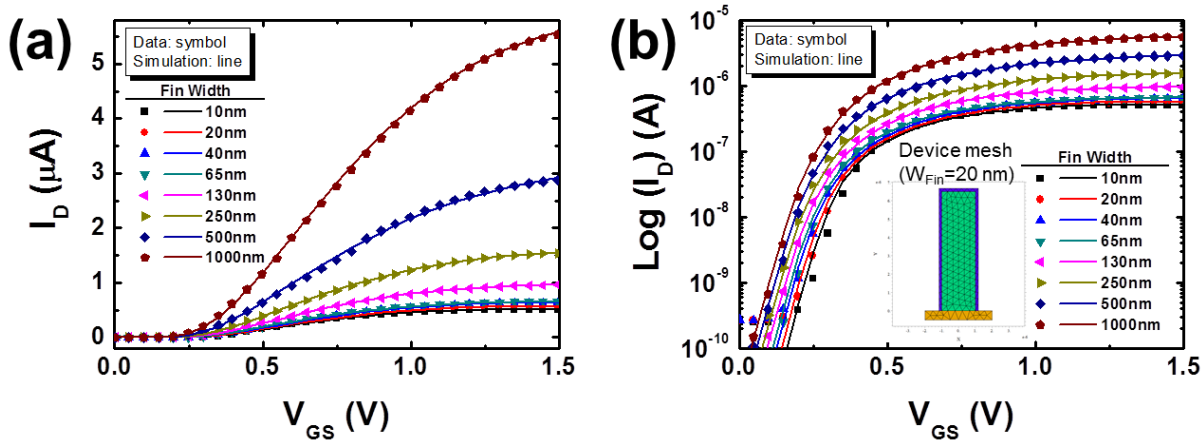


Figure 4.15 Simulation results of I_D-V_{GS} characteristics for FinFETs with the fin width (W_{Fin}) variations in (a) linear and (b) log plot. Symbols are measured data and lines are simulated curves. The inset is the meshed structure of FinFET at W_{Fin}=20 nm.

characteristics in (a) linear and (b) log plot for all devices. The detailed FlexPDE simulation script for 20 nm FinFET structure simulation is presented in an appendix III. The symbols are the measured data and the lines are the simulated curves. They are well fitted with the practical results. In detail, for W_{Fin}=20 nm, the simulations of I_D and S_{Id}/I_D^2 are shown in Figure 4.16.

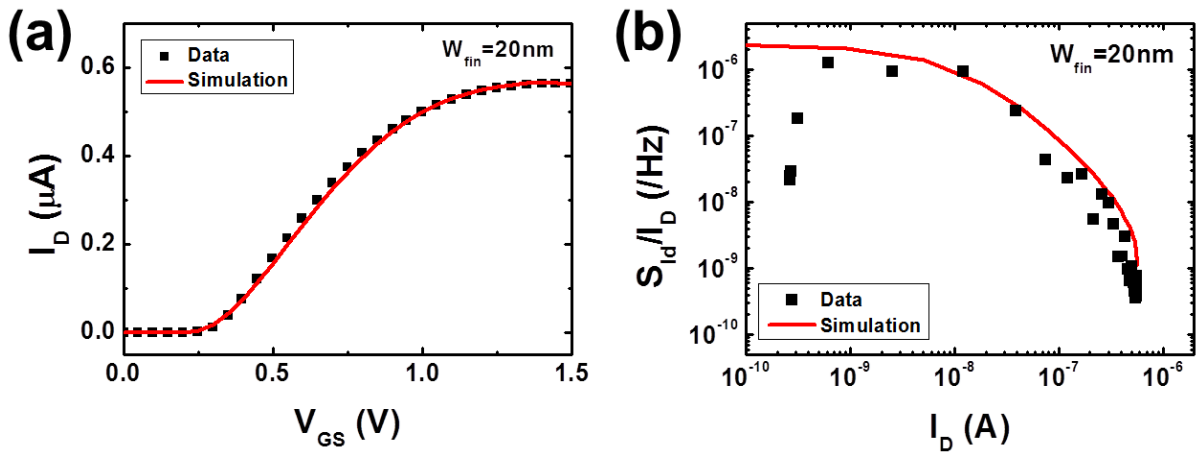


Figure 4.16 Comparison between the simulation and data of drain current and normalized drain current noise for 20 nm FinFET.

4.3 Junctionless FETs

Recently, in 2009, J. P. Colinge and his co-workers at Tyndall National Institute of University College Cork proposed a novel multi-gate structure device having no junctions between the channel and the source (and the drain), called a junctionless multi-gate transistor [141]. The basic idea started from a patent by Lilienfield in 1925 [142]. A Lilienfield device is a field-effect device like conventional MOSFETs except the one difference which is a heavily doped channel including the source and the drain. It is a resistor having a gate electrode so called 'gated resistor'. The junctionless transistor is basically equal to an accumulation-mode transistor which a channel doping concentration is same for the source and the drain.

The junctionless FET is fully depleted below threshold. If the cross section of the channel is small enough, the gate can deplete the channel entirely (i.e. off-state) due to the difference of work function between the channel and the gate electrode. Above the threshold voltage, the current flows though the bulk of silicon which is in the center of channel, and an accumulated channel can be formed if the gate voltage is increased to sufficiently large values. Therefore, it has some advantages over surface-conduction devices such as less degradation of the mobility and the near-ideal subthreshold swing [143-146]. The conduction is mainly limited by the bulk region unlike the conventional inversion-mode MOSFETs (see Figure 4.17 (c)). From the noise modeling viewpoint, the bulk conduction in junctionless FETs is expected to affect the low-frequency noise with different noise source compared to the surface conduction.

4.3.1 Device structure

The junctionless FETs in this study were fabricated on a standard Unibond® silicon-on-insulator substrate at Tyndall University, Ireland. The top silicon layer was thinned down to a thickness of 5~10 nm and the multi-gate structured nanowires were patterned by an electron-beam lithography process. The fin widths of nanowires were firstly defined 30, 40, and 50 nm. Next, a 10 nm-thick SiO_2 gate oxide was then thermally grown so that each fin width was decreased by roughly 10 nm to values of 20, 30, and 40 nm. The nanowires including channel, source, and drain were uniformly n+ doped with $1\sim2 \times 10^{19}$ cm^{-3} of doping concentration by ion implantation. For the device off-state, a p^+ poly-silicon gate electrode (the work function

is estimated about 5.25 eV) was deposited and it could be enable to make the fully depletion of channel region. The channel length for all junctionless devices is 1 μm. After the etching and oxidation process, the junctionless devices have an omega-gate structure as shown in Figure 4.17 (a). Figure 4.17 (b) and (c) shows a schematic diagram of the junctionless FETs and the cross sectional view for the bulk conduction, respectively.

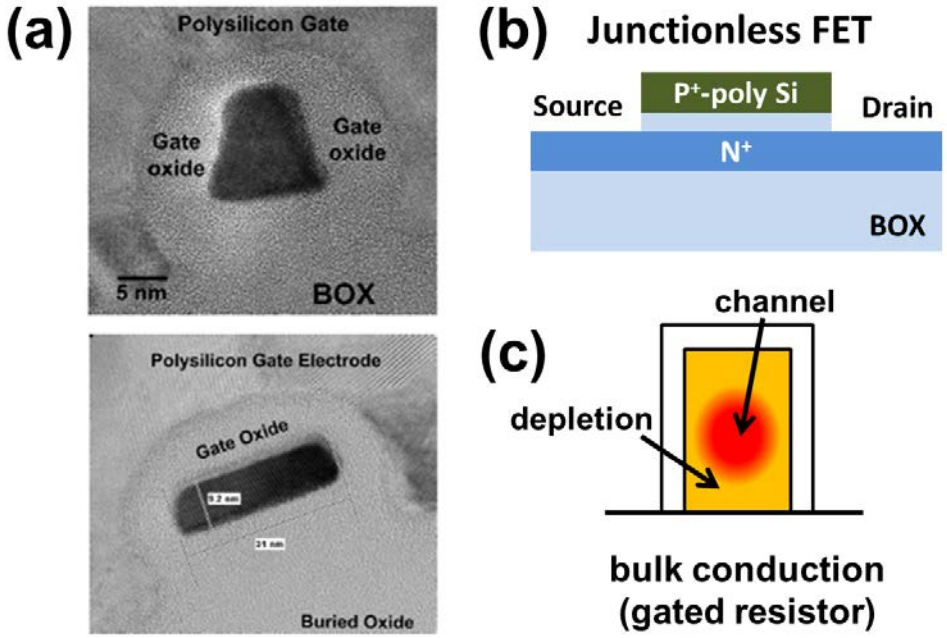
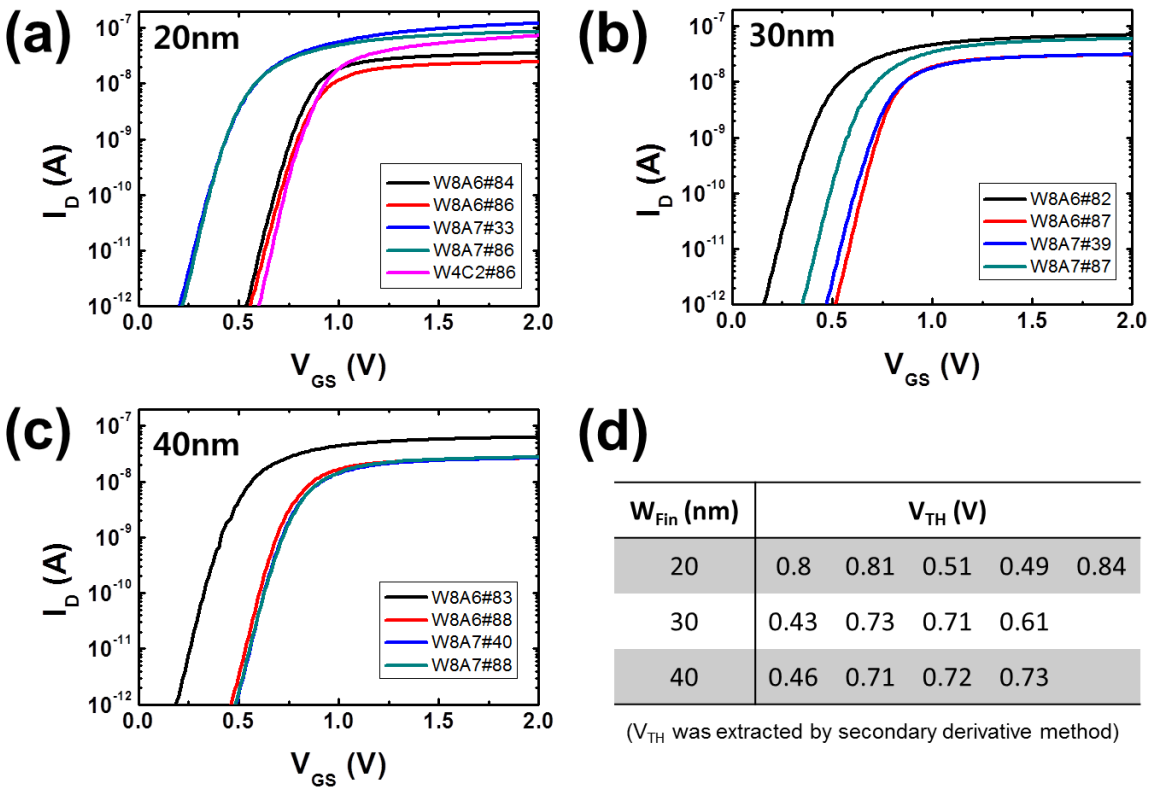


Figure 4.17 (a) Transmission electron microscope (TEM) images of junctionless multi-gate transistors. (b) Schematic diagram showing the doping profiles and (c) Electron concentration profile in the junctionless FETs having bulk conduction.

4.3.2 DC characteristics

The measurement of I_D-V_{GS} characteristics in junctionless FET were performed in a dark box at room temperature. A drain voltage of 50 mV is applied in the linear regime and the back-gate (substrate) was grounded. There are 4~5 number of devices for each different W_{Fin} and their I_D-V_{GS} characteristics are plotted in Figure 4.18 (a), (b), and (c). From the figures, a large variation for I_D-V_{GS} characteristics was observed despite of same dimension. It might be due to non-stabilized fabrication process. First of all, all devices were fabricated on a 4-inch SOI substrate having the non-uniform thickness of top silicon layer, and thereby they have different channel thickness depending on the devices. Another possible reason is the different channel cross-section mainly by e-beam lithography. The cross-sectional shape can be such as triangular, tetragonal, or distorted during the device manufacturing process. As a result, these



(d)

W_{Fin} (nm)	V_{TH} (V)				
20	0.8	0.81	0.51	0.49	0.84
30	0.43	0.73	0.71	0.61	
40	0.46	0.71	0.72	0.73	

(V_{TH} was extracted by secondary derivative method)

Figure 4.18 Typical I_D-V_{GS} characteristics of several junctionless FETs having different W_{Fin}: (a) 20 nm, (b) 30 nm, and (c) 40 nm. (d) Comparison of extracted threshold voltage depending on the samples

variations of channel dimension give rise to different transfer characteristics. The threshold voltage of all devices was extracted by secondary derivative method and compared in Figure 4.18 (d). The result is also similar to one by Y-function method.

The extracted effective mobility and subthreshold swing for all devices are summarized in Table 4.1. The effective mobility is decreased from ~150 cm^2/Vs to ~64 cm^2/Vs as increasing the fin width and the subthreshold swing is observed ~70 mV/decade regardless of the fin width. The overall value of effective mobility is somewhat lower than in the inversion-mode FETs because the junctionless FETs have heavily doped channels in which the mobility is mainly limited by impurity scattering [147].

W_{Fin}	20 nm	30 nm	40 nm
μ_{eff}	~ 150 cm^2/Vs	~ 94 cm^2/Vs	~ 64 cm^2/Vs
S	~ 73 mV/decade	~ 70 mV/decade	~ 70 mV/decade

Table 4.1 Extracted effective mobility and subthreshold swing of junctionless FETs with different fin width.

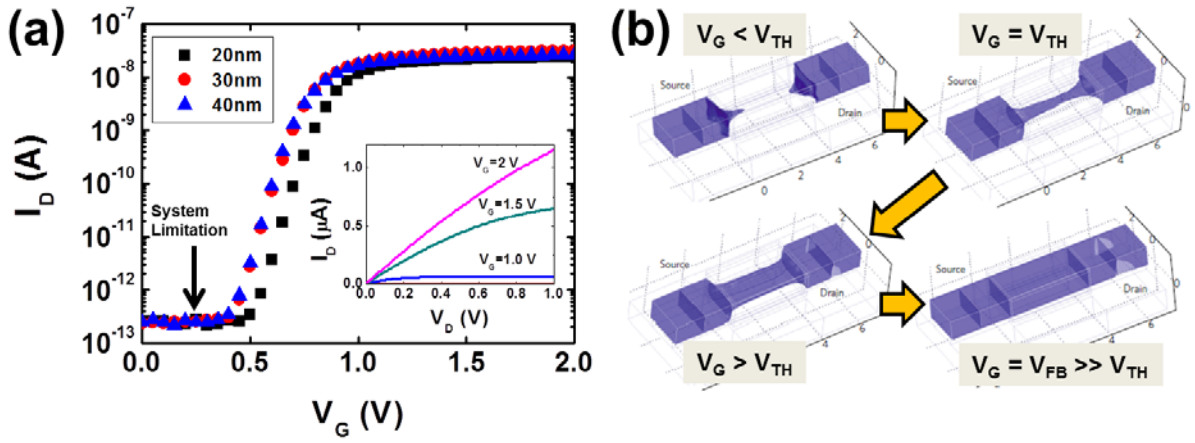


Figure 4.19 (a) I_D-V_G characteristics in log-linear plot for the junctionless FETs as changing W_{Fin}. The inset shows I_D-V_D curves as increasing V_G. (b) Electron concentration contour plot in an *n*-type junctionless FET [142].

Considering the results of threshold voltage, the specific devices having similar transfer curve for each different W_{Fin} were chosen for the width dependence as shown in Figure 4.19 (a). The inset in Figure 4.19 (a) is I_D-V_{DS} characteristics as changing of V_{GS}. As previously mentioned, the junctionless FET mainly consists of a heavily n-doped channel and a p^+ doped gate electrode and a difference of work function between the channel and the gate electrode can make a fully depleted channel for the off-state. The work function difference is seen to be the flat-band voltage (V_{FB}), which is given by

$$V_{FB} = \frac{E_{F,channel} - E_{F,gate}}{q} \tag{4.4}$$

where $E_{F,\,channel}$ and $E_{F,\,gate}$ are the Fermi-level of channel and gate electrode, respectively. The V_{FB} is estimated about 1 ~ 1.1 V. The off-state is decided according to the width of depletion layer in channel. The depletion width x_d can be expressed as

$$x_d = \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}|V_{bi}|}{qN_d}} \tag{4.5}$$

where ε_0 is the vacuum permittivity, ε_{Si} the relative permittivity of silicon, V_{bi} the built-in voltage that is also seen to be V_{FB}, and N_d the doping concentration by donors. Assuming the channel doping with 1×10^{19} cm^{-3} of a junctionless FET, the depletion width can be estimated about ~10 nm with V_{FB} from Equation 4.5. It means that the channel dimension should be roughly below ~10 nm to achieve the off-state. In the case of our devices, it is reasonable value for the device operation since the thickness of silicon layer is 5~10 nm.

When V_{GS} is increased, the depletion region in the channel is gradually removed and an

un-depleted (neutral) n^+ doped channel is formed in the center of the device. In practice, the position of un-depleted channel is a bit lower than exactly the center, but not at the bottom interface because the device structure is close to a Π-gate or Ω-gate configuration (Figure 4.17 (a)). Moreover, when V_{GS} is larger than V_{FB}, an accumulation channel is added to the total conduction. Hence, the largest part of the current in the junctionless FETs is based on the bulk conduction, but the surface conduction by the accumulation channel also contributes the total conduction at high gate voltage. Figure 4.19 (b) illustrated the channel formation of an *n*-type junctionless FET with electron concentration.

One of the advantages in junctionless FETs is a reduction of short-channel effects. The short-channel effects are secondary effects as decreasing the channel length in conventional inversion-mode transistor (n^+-p-n^+). Among them, drain induced barrier lowering (DIBL) is a well-known short-channel effect referring to a reduction of threshold voltage at higher drain voltage. It is due to the influence of the drain voltage on the barrier to electron flow at the *np* junction near the oxide surface at the source. The subthreshold current is also sensitive to DIBL. For the junctionless FET (n+-n+-n+), DIBL, which is defined as the difference in threshold voltage when the drain voltage is increased from 0.05 V to 1.0 V ($DIBL = V_{TH}(V_{DS}$=0.05 V) - $V_{TH}(V_{DS}$=1 V)), was shown in Figure 4.20.

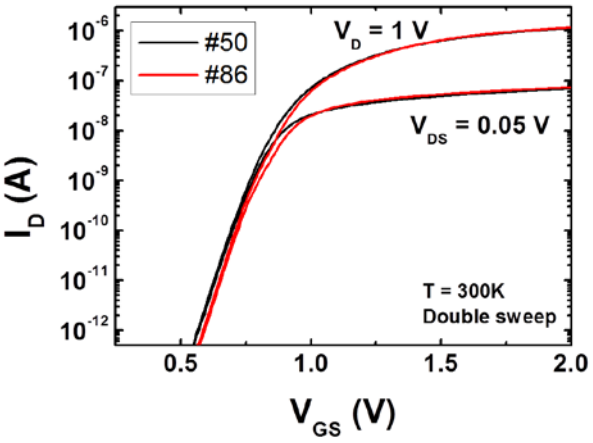


Figure 4.20 I_D-V_G characteristics of junctionless devices when V_{DS} is increased from 0.05 V to 1.0 V.

4.3.3 LF noise characteristics

4.3.3.1 Surface noise in bulk conduction

In MOSFETs, which are generally operated in inversion-mode (surface conduction), the carrier number fluctuations stem from carrier trapping/release at oxide-semiconductor interface, whereas the HMFs could prevail for bulk operated devices [111], [148], [149]. In the junctionless FET, it is previously mentioned that the conduction is dominated by the bulk in the channel. Owing to the outstanding difference of the conduction mechanism, it is

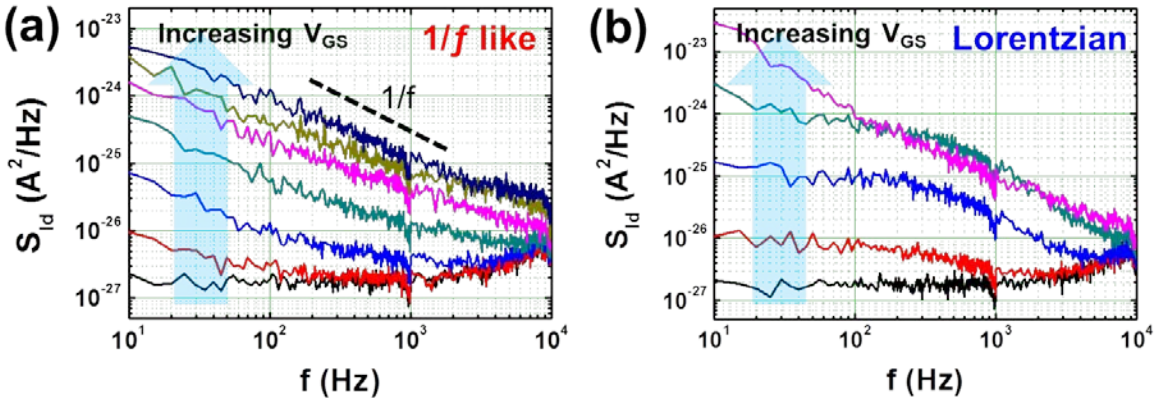


Figure 4.21 Drain current noise power spectrums (S_{Id}) as a function of the frequency for the gate voltage (V_{GS}) varying from 0.2 to 2.0 V. They exhibit (a) 1/f-like or (b) Lorentzian noise depending on the devices.

expected to have the 1/f noise originated from mobility fluctuations by the carrier scattering in the channel. However, the junctionless FET has also an additional surface conduction when the gate voltage is larger than the flat-band voltage. Moreover, it has been well known that the nanostructured devices have a large surface to volume ratio and it indicates the importance of the surface effect [150].

The drain current noise power spectrum S_{Id} of the junctionless FET was measured as changing the gate voltage from 0 V to 2.0 V between 10 Hz and 10 kHz as shown in Figure 4.21. Depending on the samples, S_{Id} was exhibited 1/*f* like (Figure 4.21 (a)) or Lorentzian (Figure 4.21 (b) behavior in subthreshold region, converging to essentially 1/*f* noise above the threshold region. Using the empirical noise model proposed by Hooge (Equation 3.10) [151], the scaling exponents for the current and frequency, β and γ were estimated to be 2 and the unity, respectively.

Drain current in junctionless FET can be defined as [143]

$$I_D = \frac{qN_C\mu_{bulk}V_{DS}}{L^2} \tag{4.6}$$

where N_C is the total number of charge carriers in the channel, μ_{bulk} the bulk mobility, and L the channel length. Based on Equation 4.6, the Hooge mobility fluctuation (HMF) model for the junctionless FET is derived as

$$\frac{S_{Id}}{I_D^2} = \frac{\alpha_H}{N_C}\frac{1}{f} = \frac{q\alpha_H\mu_{bulk}V_{DS}}{fI_DL^2} \tag{4.7}$$

To understand the origin of 1/*f* noise in the junctionless FET, S_{Id}/I_D^2 has been plotted in a log-log scale as a function of I_D as shown in Figure 4.22 (a). The noise spectrum predicted by

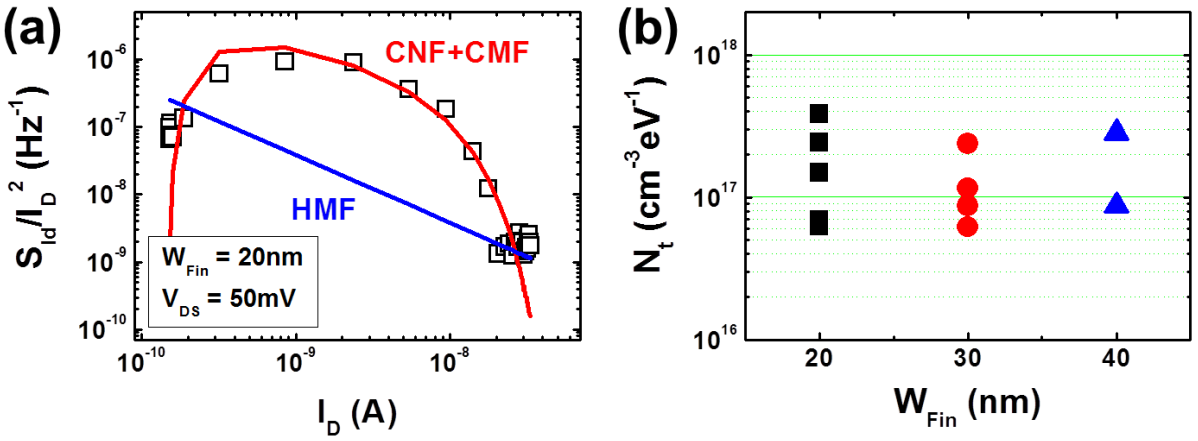


Figure 4.22 (a) log (S_{Id}/I_D^2) – log (I_D) was compared with the CNF+CMF and HMF model for W_{Fin}=20 nm. (b) Extracted volume trap density N_t of junctionless FETs with different W_{Fin}.

the number fluctuations with correlated mobility fluctuations (CNF+CMF) model which is verified over a large current range, both below and above threshold. The noise predicted by the HMF model is also shown by the straight dashed line but it is obviously not able to explain the low-frequency noise dependence on the drain current from below to above threshold. Therefore, Figure 4.22 (a) clearly indicates that the noise in junctionless FETs is affected by trapping/release of carriers even though the conduction takes mostly place in the bulk of the devices.

Based on the CNF+CMF model, the volume trap density N_t and the Coulomb scattering coefficient α_C can be calculated, providing the information on the quality of the oxide interface and the correlated mobility fluctuations by the trapped charges, respectively (Figure 4.22 (b)). The extracted N_t are from 6×10^{16} to 3×10^{17} $cm^{-3}eV^{-1}$ with applying oxide tunneling length $\lambda = 1\times10^{-8}$ cm for the silicon dioxide [102]. These are similar to those typical in state of the art bulk transistors and considerably smaller than in high-*k* MOSFETs where $N_t=10^{19}$ ~ 10^{20} $cm^{-3}eV^{-1}$ [113], [152], [153]. The value of α_C ranges from 1.1×10^4 to 5.1×10^5 Vs/C, indicating that correlated mobility fluctuations play an important role in the high current region [87]. It can be assumed that these mobility fluctuations are due to Coulombic scattering by charged traps.

4.3.3.2 Schottky-Read-Hall recombination

Despite of the good interpretation of the CNF+CMF model for the junctionless FETs, it is difficult to understand the effect of traps at the oxide-semiconductor interface in subthreshold

region. Because the silicon-gate oxide interfaces are depleted in that regime, and the conduction path is in the center of the nanowire, away from the gate oxide interfaces. A possible explanation is the fluctuation of the channel thickness in subthreshold when the device is partially depleted. This effect arises from the presence of Shockley–Read–Hall (SRH) generation/recombination centers in the Debye transition region between the neutral channel and the depletion region [154]. This effect has been also observed in junction FETs or in four-gate FETs (G4-FETs) [155], [156].

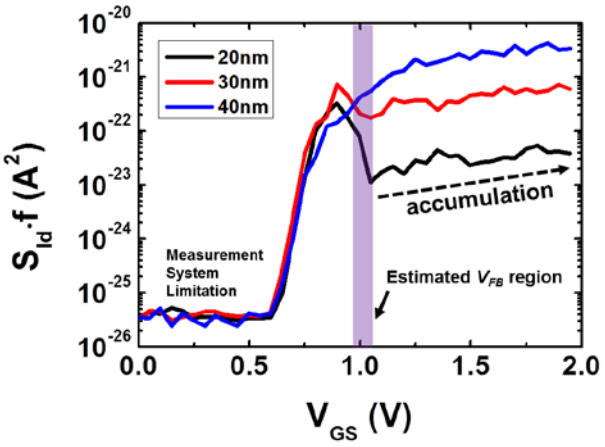


Figure 4.23 Drain current noise power (S_{Id}·f) as a function of the gate voltage at V_{DS}=50 mV.

The fluctuations of depleted region can give rise to the generation-recombination (g-r) noise that is characterized by a Lorentzian spectral distribution. When the noise power (=S_{Id}·f) plotted as a function of V_{GS}, the g-r noise component reaches a peak near threshold as shown in Figure 4.23 [157], [158]. When V_{GS} is larger than V_{FB}, on the other hands, the depletion region disappears which will decrease the g-r noise in spite of the presence of a surface accumulation channel [159]. The accumulation channel contributes to the total noise as a result of fluctuations at the oxide-semiconductor interface. The peak at threshold disappears in wide devices, which might be due to the larger size of the bulk conduction region. In Figure 4.24 (a), low-frequency noise by the depletion and accumulation are compared for the different values of drain voltage. At V_{DS}=50 mV, the noise power increases as the square of drain current below the threshold, however, it rises again for large gate voltages after the small reduction of noise, as it does in Figure 4.24 due to conduction in the surface accumulation. Such behavior is not observed for the case of V_{DS}=1 V because there is only partial depletion of the silicon near the drain and no accumulation layer is formed near the drain. Hence, the noise originating from the surface conduction could not be observable.

In conclusion, the low-frequency noise in junctionless FETs was well explained by the CNF+CMF model indicating the trapping and de-trapping of charge carriers. The junctionless FET exhibits two kinds of noise sources as far as CNFs are concerned: one is due to channel thickness fluctuations in the depletion region and the other is due to carrier concentration fluctuation at the oxide-semiconductor interface in the accumulation region. The relative

contribution of the noise sources in junctionless FETs might be a diagnostic index for the quality of the junctionless FETs such as the uniformity of the line width of the channel.

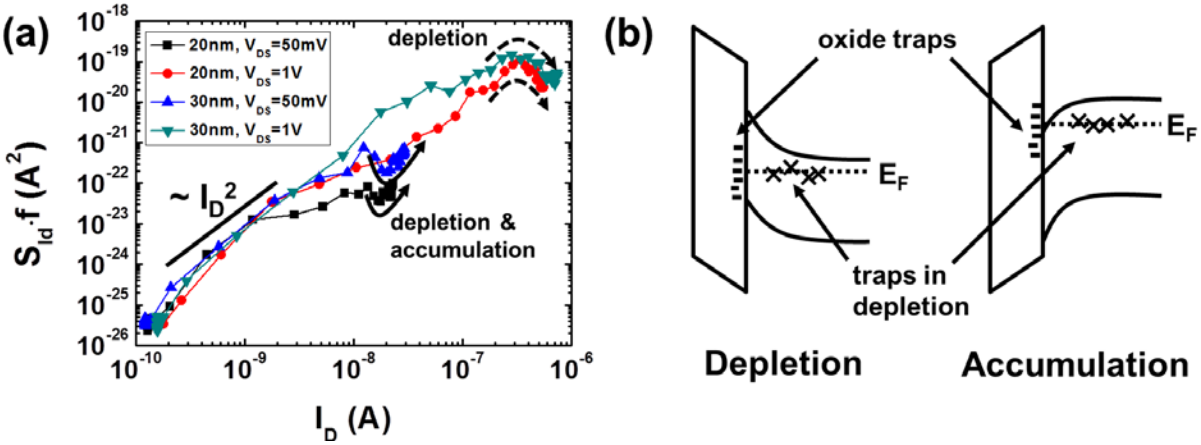


Figure 4.24 (a) Drain current noise power as a function of the drain current for the drain voltage is 50 mV and 1 V. (b) Schematic for the influence of traps at the oxide-semiconductor interface and in depletion region according to the conduction mode.

4.4 Summary: Surface vs. Bulk conduction

From chapter 4.2 and 4.3, the electrical and LF noise properties were studied for the multi-gate structured FETs. In the FinFET, the conduction arises at the oxide-semiconductor interface, i.e. the surface conduction and their transport and LF noise are influenced by the surface effect. In contrast, the junctionless FET has a similar structure to the FinFET but its conduction is limited by the bulk region, i.e. the bulk conduction. The electrical behaviors and LF noise are not seriously affected by the surface. For LF noise characteristics, both devices appear in the shape of 1/*f* noise but their different noise origin turns out. In Figure 4.25, I_D-V_{GS} and LF noise characteristics are experimentally compared with similar geometric device size for both devices. The I_D in the FinFET has much larger than the junctionless FET but the current suppression is observed at high current due to the surface roughness. It proves that the bulk conduction in the junctionless FET becomes free from the surface roughness effect compared to the FinFET.

Similarly, LF noise in the junctionless FET is expected to originate from the mobility fluctuations but it is not. As shown in Figure 4.25 (b), the LF noise behaviors are compared as changing the drain current (left) and the gate voltage (right). Both devices are well understood with the number fluctuations model (concretely, CNF+CMF model) due to the trapping and de-trapping of charge carriers at the semiconductor-oxide interface. Using Equation 3.28, the mobility fluctuation coefficient α_C was extracted to 1.7×10^3 and 3.8×10^4 Vs/C for the FinFET and the junctionless FET, respectively. A relatively large value of α_C in the junctionless FET indicates larger Coulomb scattering of charge carriers. These mobility

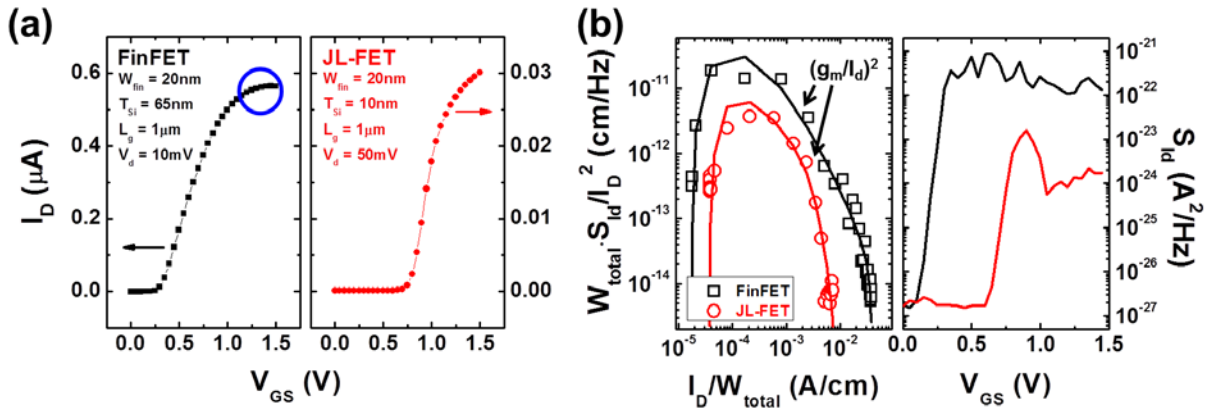


Figure 4.25 (a) Transfer characteristics of the FinFET and junctionless FET. (b) Left figure is the total width normalized noise as a function of the current. A solid line is a fitting curves as $(g_m/I_D)^2$. Right one is drain current noise variation for the gate voltage.

fluctuations might be due to the traps near the Si/SiO_2 interface and/or in the depletion region of junctionless FET channel even if the silicon oxide typically has lower trap density than high-k materials. For the volume trap density N_t, the FinFET has about 8.3×10^{18} $cm^{-3}eV^{-1}$ whereas the junctionless FET has 1.2×10^{17} $cm^{-3}eV^{-1}$. The FinFET has one order of higher than the junctionless FET but is rather smaller compared to conventional high-k devices. In spite of same interpretation by the carrier number fluctuation model for both devices, the noise behaviors are different. As shown in the right plot of Figure 4.25 (b), for the FinFET, S_{Id} gradually decreases as increasing V_{GS}. It represents a relationship between S_{Id} and the current saturation due to the surface effect. On the other hand, the junctionless FET exhibits a noise peak near the threshold voltage that is related to the g-r noise due to the Schottky-Read-Hall generation-recombination. Afterward, the drain current noise increases again as increasing V_{GS} with the formation of accumulated channel at the surface.

In conclusion, the role of the conduction mechanism for LF noise is investigated with the electrical and noise analysis in multi-gate structure FETs. LF noises in both devices are well explained with the CNF model but it turns out that the origin is different. In the FinFET, the LF noise is originated from the carrier trapping and de-trapping at the oxide-semiconductor interface as in the case of conventional inversion mode transistors. However, in the junctionless FET, it might be due to the charge generation-recombination on the boundary between the channel region and depletion region. For the better understanding, the different noise mechanisms in the FinFET and the junctionless FET are illustrated in Figure 4.26.

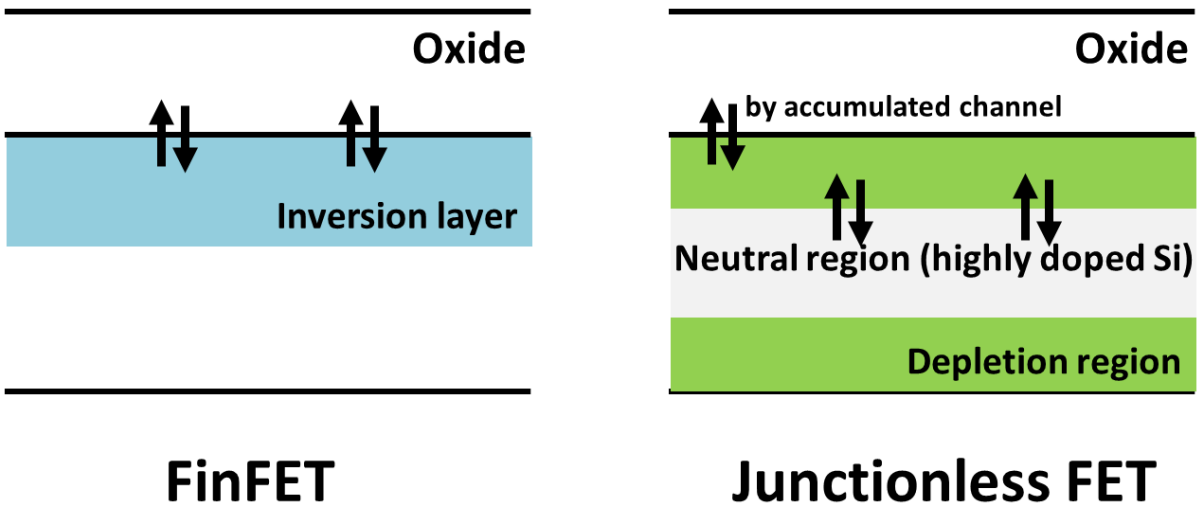


Figure 4.26 Schematic illustrations for the trapping and de-trapping of charge carriers in the FinFET and the junctionless FET.

Chapter 5 Nanowire and Nanotube

5.1 Background: Toward 1-D structures

Recently, from conventional state-of-art Si CMOS technology, one-dimensional structures (1-D) or nanostructures defined as having at least between 1 and 100 nm have received great interests owing to their peculiar and fascinating properties, and applications. The interesting phenomena are, for instance, size-dependent excitation [160-162], ballistic transport [163], Coulomb blockade [164-166], and metal-insulator transition [167] that are associated with their nano-scale size. Also, the quantum confinement of electrons by the potential wells of 1-D structures provides the opportunity to control the electrical, optical, magnetic, and thermoelectric properties in solid-state materials [168]. In addition to these physical potential in 1-D structures, their smaller size can effectively contribute for the large scale integration and low-power consumption. However, there are still difficulties for the applications. Indeed, based on bottom-up nanostructures, a lack of appropriate large-scale integration techniques has been an obstacle and the top-down nanostructures have complexities for manufacturing process. Nevertheless, many studies have been continued using 1-D structures from the perspectives between top-down and bottom-up approaches.

5.2 3-D stacked Si and SiGe nanowires

Based on top-down approach, Gate-all-around (GAA) nanowire (NW) transistors are promising candidates in the advanced MOS technology. They offer several advantages such as improved electrostatic performance overcoming the short channel effects with a better integration density due to the three-dimensional (3-D) stacking structure [169-171]. Moreover, the device performance can also be enhanced by introducing structural strain. Indeed, in compressively strained (c-strained) SiGe NWs, the hole mobility

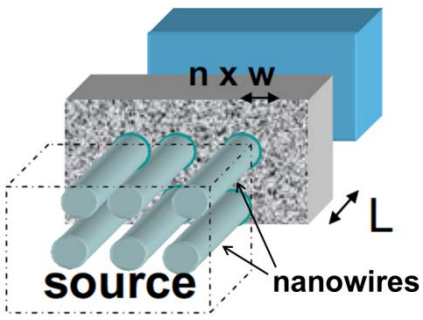


Figure 5.1 3-D view of stacked gate-all-around (GAA) nanowire FETs [169].

increases by reducing both the effective hole mass and the inter-sub band scattering [172], [173]. However, GAA NW devices could suffer from the higher impact of interface quality on their operation due to the larger interface/volume ratio compared with planar structures [40]. Low-frequency noise is a powerful technique to characterize the electronic devices, providing relevant information about the defect density in the active regions [174]. Very few studies have been dedicated to LF noise in Si NWs [175-177].

In the section “3-D stacked Si and SiGe nanowires”, the electrical properties and low-frequency noise characterization of high-*k*/metal gated 3-D stacked Si (NMOS) and SiGe (PMOS) nanowire transistors coming from the CEA-LETI (France) will be presented. They were fabricated based on the top-down technology as a combination of anisotropic and isotropic etchings during gate patterning. To improve the device performance, some devices were applied the channel strain or annealed by H_2 gas.

5.2.1 Mobility enhancement – strain effect

Recently, the output current of a MOS device which determines the device performance is getting smaller as decreasing the device size and it is limited by some physical limitations such as off-state leakage current and power density. To continue CMOS device performance improvement with device scaling, the mobility enhancement technique is concerned starting with the 90-nm technology generation [178-180]. The mobility enhancement technique is that applying physical stress induce the appropriate strain in the channel region of devices increases both electron and hole mobilities in the strained channel [181]. The physics of strained Si or SiGe can be figured out with the carrier mobility which is given by

$$\mu = \frac{q\tau}{m^*} \tag{5.1}$$

where q is the electronic charge, $1/\tau$ the average scattering rate, and m^* the effective mass of semiconductor. The physical mechanism of strain is that the mobility is improved by reducing the effective mass and/or the scattering rate [182]. For electrons, both changes of effective mass and scattering are generally accepted as important for the mobility enhancement [183] but only effective mass change due to band warping plays a significant role for hole [184].

There are two techniques for the implementation of strain on MOSFETs [185]. A global strain technique is by inducing the stress across the entire substrate and a local strain technique is engineered into the device by means of epitaxial layers and/or high-stress nitride

capping layers. There are some local techniques such as the Contact Etch Stop Liners (CESL) and the uniaxial stress induced by source and drain stressors. First works on strained Si MOSFETs has focused on biaxial stress using a substrate but the industry is adopting process induced uniaxial stress. Because the uniaxial stress can be pursued larger hole mobility enhancement at low strain and smaller threshold voltage shift [184]. To realize the strain, Si and Ge are generally used for a full range of composition with the lattice mismatch of ~4.2 % [186]. When a $Si_{1-x}Ge_x$ thin film having a larger lattice constant is grown on a Si substrate with smaller constant, the $Si_{1-x}Ge_x$ film retains the in-plane lattice constant of the substrate and is under a biaxially compressive strain as shown in Figure 5.2 (a). In addition, there is a band offset of ~7 meV/Ge% between the strained $Si_{1-x}Ge_x$ film and the relaxed Si substrate and the band diagram is illustrated in Figure 5.2 (b) [187]. The band offset exists typically on valence bands, thereby the hole mobility will be improved. The reason why improve the hole mobility in c-strained SiGe devices is due to an energy gap between heavy hole and light hole band energies and it induces band mixing. This leads to smaller hole effective mass in the lower energy band and reduced inter-band scattering between the two mixed bands [188].

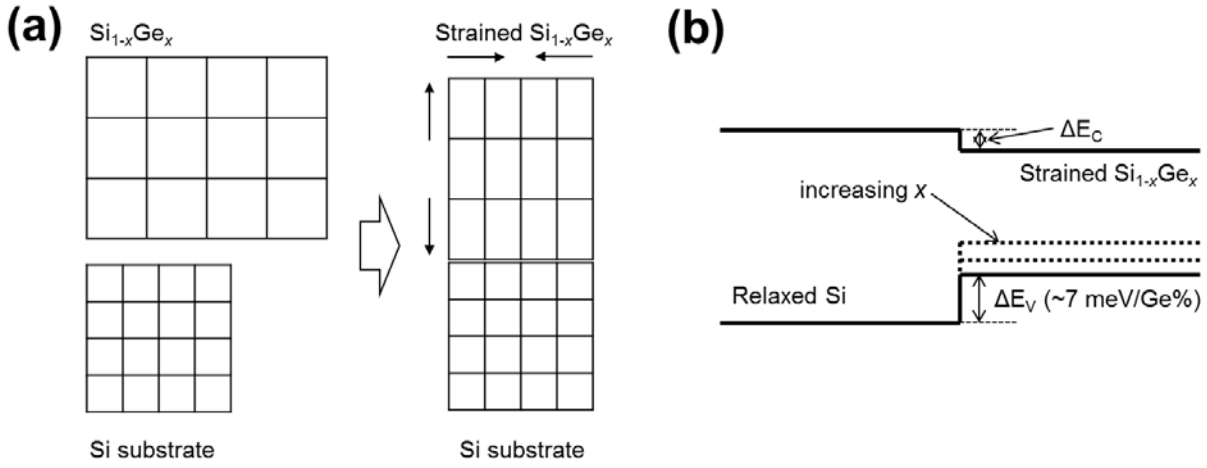


Figure 5.2 (a) Schematic diagram of lattice arrangement of the strained $Si_{1-x}Ge_x$ grown in Si substrate and (b) the corresponding band alignment. As increasing *x* (i.e. % of Ge) in $Si_{1-x}Ge_x$ film, the band offset is increased with a ratio of ~7 meV.

For the mobility enhancement by the strain, the influence of dopant diffusion should be also considered. In practice, the c-strained SiGe is used for *p*-type transistors due to higher hole mobility and a major dopant in *p*-type devices is Boron. In the case of Boron, the relaxed (i.e. tensile) SiGe increases the diffusion coefficient while the c-strained one retards it since the presence of Ge increase the concentration of both vacancies and interstitials and dopants

are expected to diffuse faster in relaxed SiGe layers [189-192]. It can affect several device parameters such as the threshold voltage shift or the subthreshold swing [193].

5.2.2 Device structure

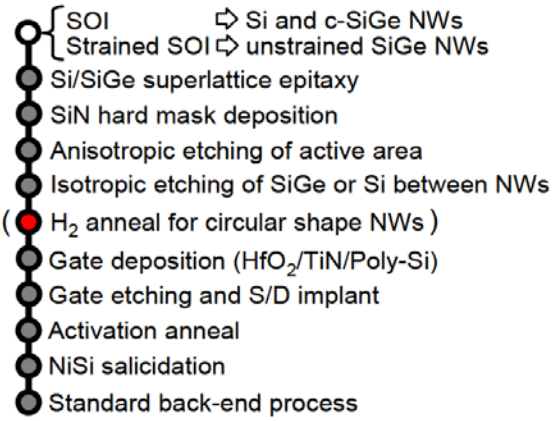


Figure 5.3 Process flows of 3-D stacked Si and SiGe nanowires. H_2 annealing is performed at 750 °C.

3-D stacked Si (NMOS) and SiGe (PMOS) nanowire transistors with high-k/metal gate stacks were fabricated in CEA-LETI (France) by K. Tachi et al [194]. The process flow of 3-D Si and SiGe nanowire devices is shown in Figure 5.3. For Si and c-strained SiGe nanowire transistors, SOI (001) wafers were used while tensile-strained (1.3 GPa) SOI (001) wafer were used for un-strained SiGe ones. $Si/Si_{0.8}Ge_{0.2}$ superlattices were epitaxially grown on the wafers by the reduced pressure chemical vapor deposition. After SiN hard mask layer deposition, a hybrid deep ultraviolet/e-beam lithography and resist trimming were combined to define narrow lines. A damascene process was used; cavities were patterned by anisotropic dry plasma etching with various lengths. The same reactive ion etching reactor was used to remove the Si (or SiGe) isotropically. A 2 nm thickness of Si capping layer was grown at 650 °C on the liberated SiGe nanowires to achieve higher mobility. An HfO_2 (3 nm) / TiN (10 nm) / Poly-Si gate stack was sequentially

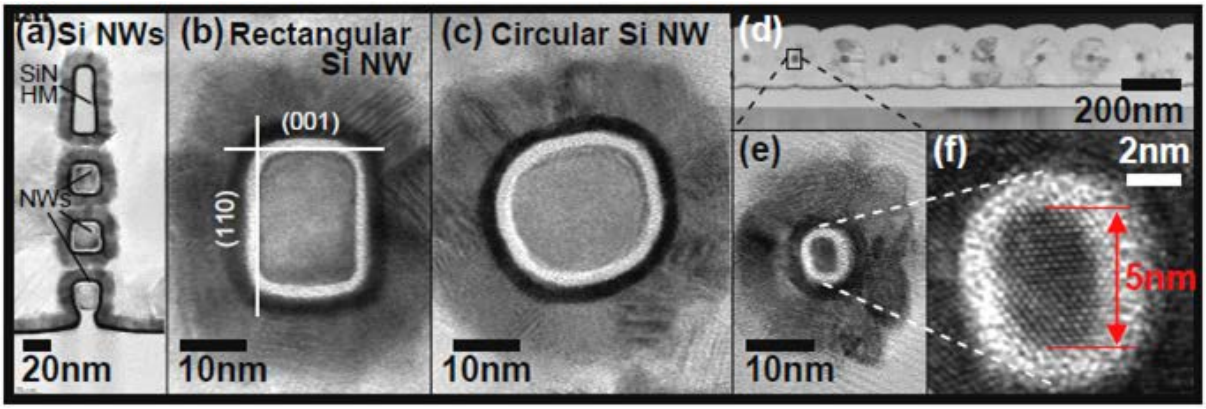


Figure 5.4 Cross-sectional TEM images of 3-D stacked Si nanowire transistors with high-*k*/metal gate stacks; (a) 3-D stacked nanowires, (b) enlarged image of a rectangular nanowire, (c) a circular nanowire by H2 annealing, (d) regularly arrayed 5nm-diameter transistors, and (e) detailed 5nm nanowire. The crystalline quality of those circular nanowires is confirmed by high-resolution TEM image in (f).

deposited on nanowires. The gate is overlapped on source/drain (S/D) regions which have SiN hard masks on top of the Si/SiGe superlattices. After the gate patterning, the S/D implantation (Boron doping, 10^{20} cm^{-3}), the spacer formation, and the top of S/D were silicided for the activation of the dopants. The fabrication was completed with a standard back-end of line process. Figure 5.4 shows a representative cross-sectional transmission electron microscopy (TEM) picture of 3-D stacked Si nanowire transistors with high-k/metal gate stacks.

For SiGe nanowires, the cross-sectional shape as shown in Figure 5.5 was hexagonal with {111} facetted sidewalls most likely due to the thermal budget used during the Si capping layer formation. It is also notable that a lower-*k* SiO_2-like interfacial layer (TIL: 1.5 ~ 2 nm) grew because of the non-optimized thermal process. For the long-channel devices, the channels of c-strained nanowires were bended (Figure 5.5 (c)) whereas the short-channel SiGe ones are straight (Figure 5.5 (d)). On the other hand, the cross-sectional TEM images of un-strained SiGe were shown in Figure 5.5 (f), (g), and (h). According to the comparison of Figure 5.5 (b) and (h), the c-strained nanowires have more {111} facetted sidewalls than un-

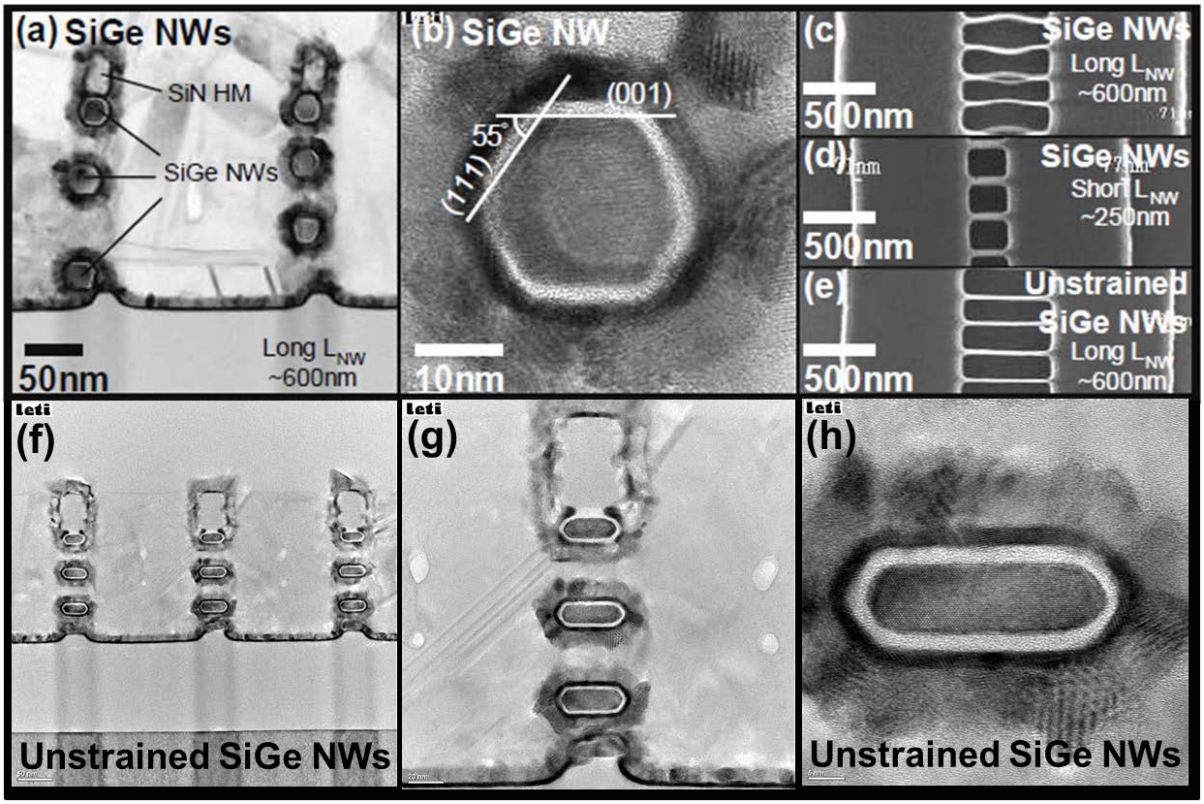


Figure 5.5 (a) Cross-sectional TEM images of 3-D stacked compressively strained (c-strained) SiGe nanowires and (b) enlarged images of one nanowire. Top-view of c-strained SiGe nanowire with (c) L=600 nm and (d) L=250 nm compared with (e) long-channel un-strained nanowires. Cross-sectional TEM images of un-strained nanowires are in (f) ~ (h).

strained ones. But, in here, the effect of different orientation is not addressed. For all devices, total number of nanowires has 150 nanowires in parallel (3 × 50 = 150 wires). So, total width for c-strained and un-strained devices is estimated about 12.008 and 12.320 μm, respectively.

5.2.3 C-strained and un-strained SiGe nanowire *p*-type FETs

5.2.3.1 DC characteristics

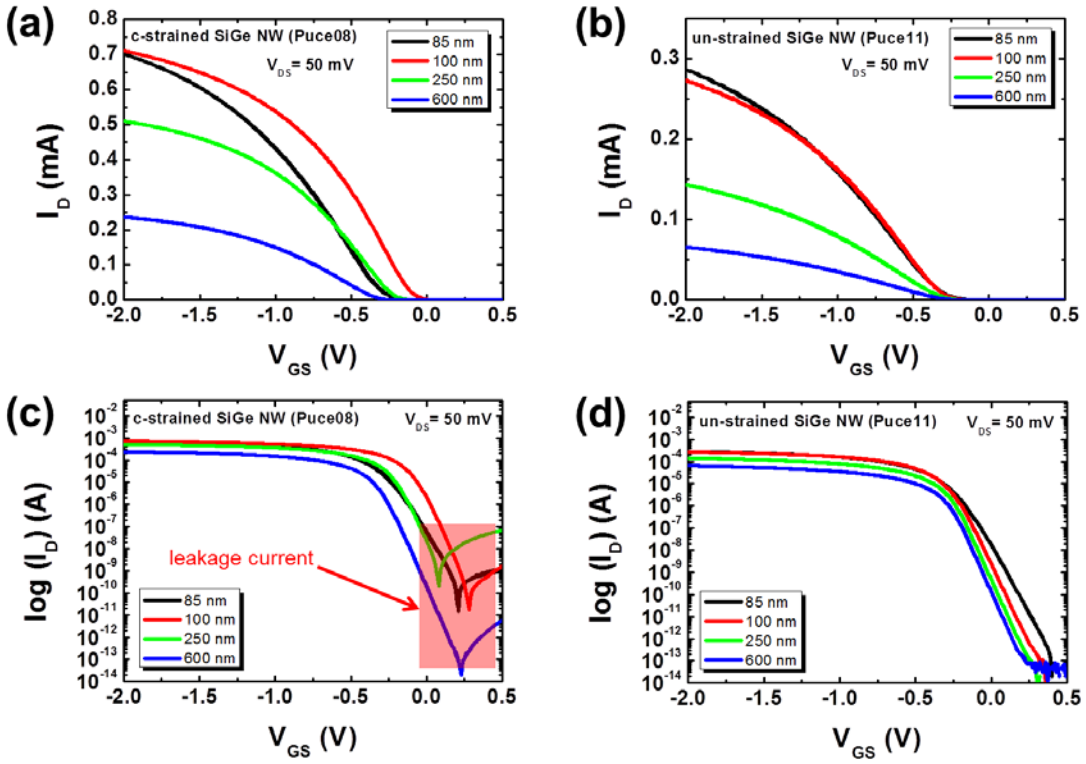


Figure 5.6 Typical I_D-V_{GS} characteristics of c-strained and un-strained SiGe core-shell nanowire *p*-type transistors with different channel lengths. Linear plots: (a) and (b) and Log plots: (c) and (d). For the c-strained SiGe devices, large gate leakage currents were observed whereas there were no leakage currents in un-strained SiGe ones.

Typical I_D-V_{GS} characteristics of c-strained and un-strained SiGe nanowire *p*-type FETs with different channel lengths are shown in Figure 5.6 (a) and (b). The drain currents of c-strained SiGe devices are much larger than those of un-strained SiGe ones since the compressively strain improve the hole mobility in SiGe. As decreasing the channel length, the drain current is generally increased but both device of 85 nm channel length appears different behavior. The transfer curves were also drawn in log (I_D)-V_{GS} plot in Figure 5.6 (c) and (d) and large gate leakage currents in c-strained SiGe devices were observed.

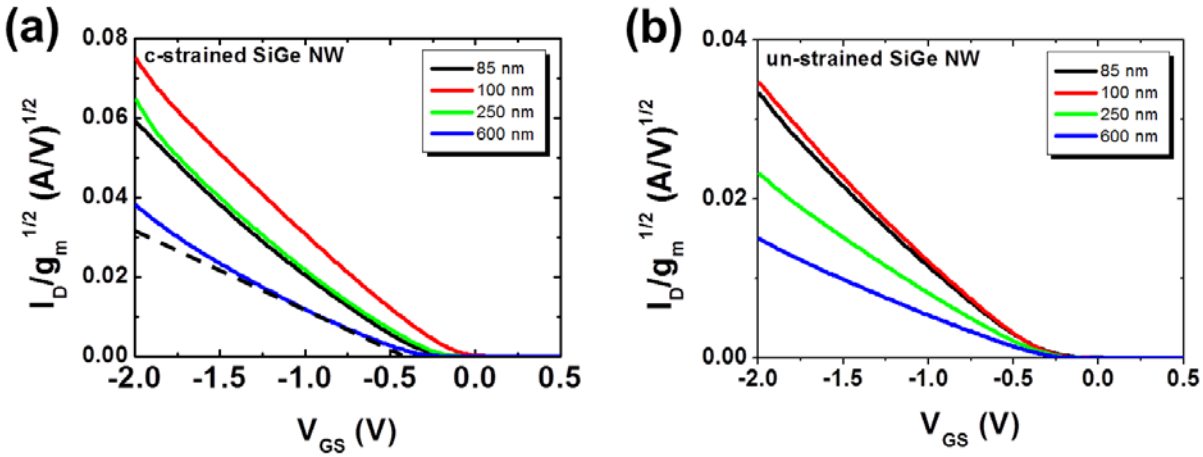


Figure 5.7 $I_D/g_m^{1/2}$ characteristics as a function of V_{GS} using Y-function method.

The impact of strain on threshold voltage (V_{TH}) and low field mobility (μ_0) parameters was analyzed using the Y-function method [46]. Each Y-function ($=I_D/g_m^{1/2}$) of both devices was shown in Figure 5.7. The non-linearity of Y-function was observed for all devices owing to the strong impact of the surface roughness (i.e. θ_2 effect as shown in Equation 2.23) on the electrical transport in thin gate oxide MOSFETs [195-197]. Instead of non-consideration of θ_2 effect, herein the results of extracted V_{TH} from Y-function method were compared with the secondary derivative method. As shown in Figure 5.8, the voltage difference of V_{TH} between both methods ($|\Delta V_{TH}| = V_{TH,\ Y\text{-}function} - V_{TH,\ second\ derivative}$) is about 50 mV and it can be negligible. The V_{TH} is around -0.3 V, showing V_{TH} roll-off for the c-strained SiGe NWs [198], [199]. However, no V_{TH} shift was observed for all channel un-strained devices. For the low-field mobility, the extracted values of the c-strained SiGe NWs is in the range of 110 ~ 120 cm^2/Vs, which is three times higher than in the un-strained SiGe NWs, where μ_0 = 40 ~ 50 cm^2/Vs. In the same way, using the Y-function method, the series resistance and effective length were also estimated. The values of series resistance for the c-strained and un-strained SiGe NWs are about ~150 Ω and ~250 Ω, respectively. Hence, the series resistance is small enough and any effective effects from the series resistance were not observed for the noise analysis.

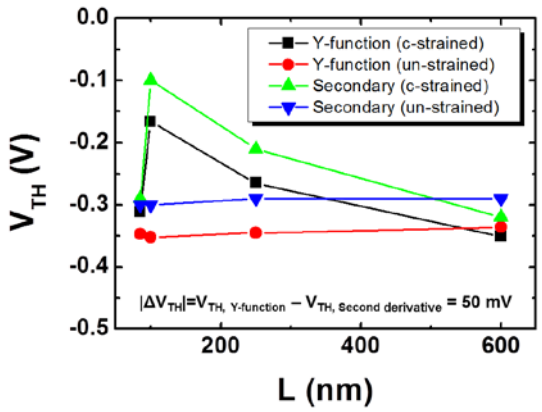


Figure 5.8 Comparison of extracted threshold voltages by the Y-function and secondary derivative method.

Using the Y-function method, the effective channel length ($L_{eff} = L - \Delta L$) was calculated as shown in Figure 5.9. $1/G_M$ defined with β from Equation 2.28 as [196]

$$\frac{1}{G_M} = \frac{L - \Delta L}{W \mu_0 C_{OX}} \tag{5.2}$$

where ΔL is - 42±5 and - 8±5 nm for c-strained and un-strained SiGe devices, respectively. But the points of $1/G_M$ in 85 nm devices strayed from the linear fit. According to the unusual results of previous MOS parameter extractions such as the threshold voltage, low-field mobility, and effective channel length, the 85 nm length devices were decided that the devices have some errors in here. Hence, it was disregarded for the noise analysis. And the subthreshold swing (*SS*) for all gate lengths was calculated and they are around 69 mV/decade for all c-strained devices, whereas *SS* ≈ 80 mV/decade for 100 nm un-strained SiGe NWs, indicating that GAA NW transistors effectively sustain short channel effects.

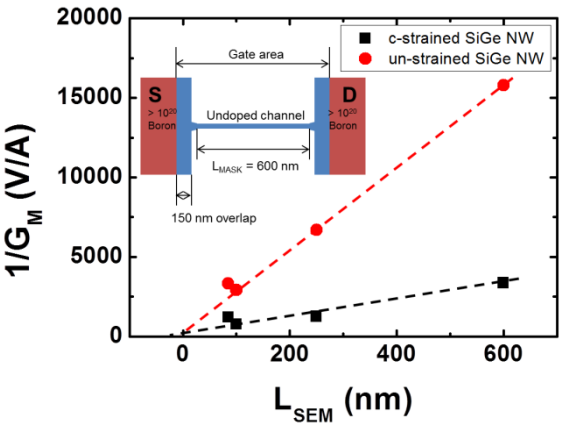


Figure 5.9 Effective length extractions for c-strained and un-strained SiGe NWs. The inset indicates the gate area of device.

5.2.3.2 Capacitance behaviors on the strain effect

The channel strain effect between the c-strained and un-strained SiGe NWs is confirmed using the split *C-V* measurement. To observe the variation of the inversion charge density Q_i, the gate to channel (connecting to source and drain) capacitance C_{GC} was measured. The oscillation frequency and level are fixed at 1 MHz and 50 mV, respectively. For the c-strained SiGe NWs, a significant hump exists in the *C-V* curves as the gate voltage is swept from the accumulation to inversion whereas the un-strained ones have rather not showing up. Figure 5.10 exhibits the clear differences between both devices with C_{GC} differentiated by the gate voltage. For the hump in *C-V* curves, there are two kinds of possible explanations. One is due to the carrier (in here, hole) confinement phenomenon induced by the band gap discontinuity where holes are confined between the Si cap and strained SiGe heterostructure. Another is due to the traps located at the heterointerface. It is not clear which one is the origin but the obvious difference between the c-strained and un-strained SiGe NWs with Si capping layer is observed with the *C-V* measurement.

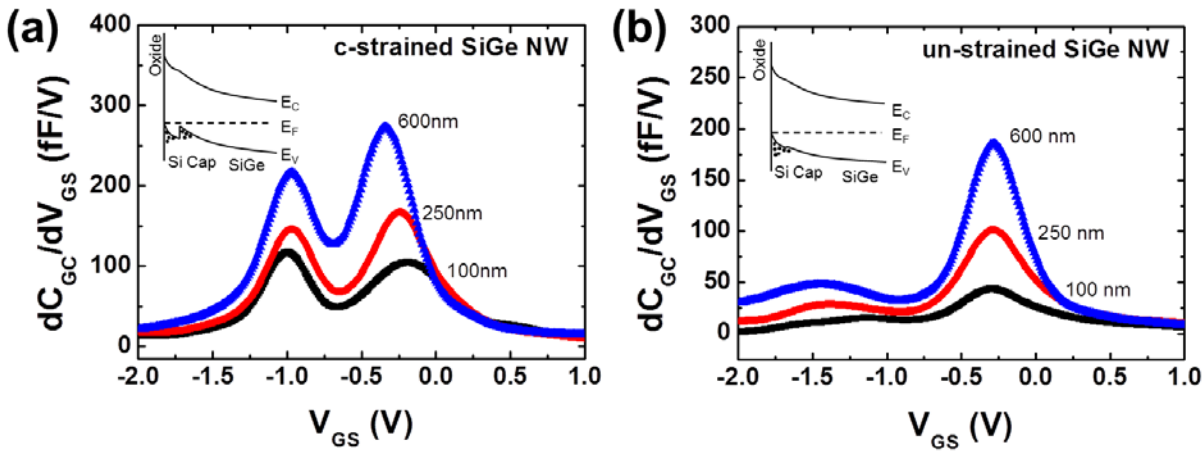


Figure 5.10 C_{GC} differentiated by V_{GS} for the (a) c-strained and (b) un-strained SiGe NWs with Si capping layer. Insets are simple schematic diagram for the band structure. C-strained SiGe NWs appears explicit hump due to the strain effect compared to the un-strained ones.

5.2.3.3 Inhomogeneous oxide trap distribution

To analyze the noise properties between the c-strained and un-strained SiGe NWs, the low-frequency (LF) noise measurements were performed between 10 Hz and 10 kHz at fixed drain voltage of 50 mV. Their typical drain current noise spectra between the c-strained and un-strained devices are compared between 600 and 100 nm channel length. As shown in Figure 5.11, for the 600 nm c-strained SiGe NWs, the spectrum shows non-1/*f* behavior (close to Lorentzian behavior) in the subthreshold and near threshold region whereas the un-strained and the 100 nm c-strained devices appeared obviously 1/*f* behaviors for the whole region apart from the channel strain. Based on the Hooge empirical relation (Equation 3.10), the drain current noise spectrum is proportional to the reciprocal frequency with the exponent γ as

$$S_{Id} \propto \frac{1}{f^{\gamma}} \tag{5.3}$$

where the exponent γ is normally the unity for 1/*f* noise and it can be extracted from the slopes of current noise power spectrum. All extracted values of γ of all SiGe NWs were extracted as changing the gate voltage and shown in Figure 5.12. The large variations of γ were observed in the c-strained SiGe NWs especially for 250 and 600 nm channel length but short-channel c-strained (85 and 100 nm) and un-strained devices were not shown. Below 100 Hz, the γ is smaller than the unity whereas it is larger above 1 kHz. It might be due to the

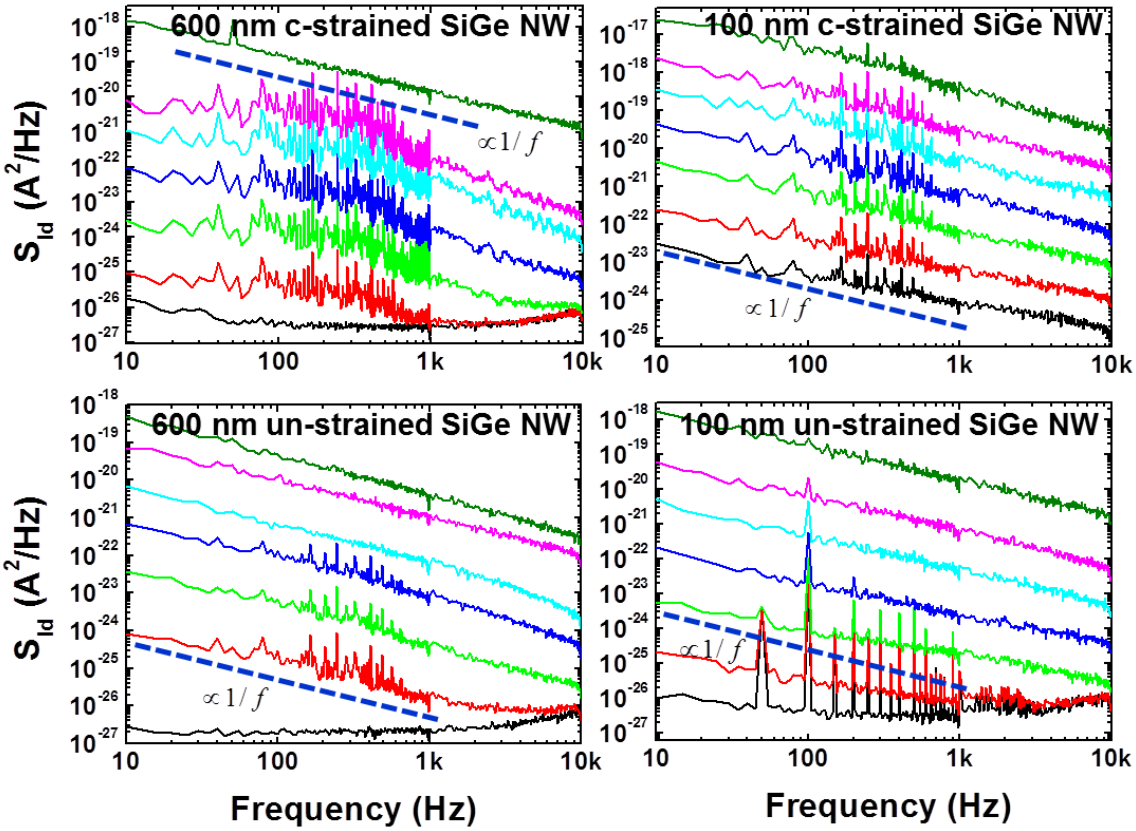


Figure 5.11 Comparison of drain current noise spectra between the c-strained and un-strained SiGe NWs.

physical channel bending for the long-channel c-strained SiGe NWs coming from the strain effect. The evidence of channel bending can be confirmed by SEM images in Figure 5.5 (c), (d), and (e). In Figure 5.5 (d), for the 250 nm c-strained SiGe NWs, the bending is invisible to the naked eye but it is predicted that there is weak physical bending to affect the frequency dependence on the noise.

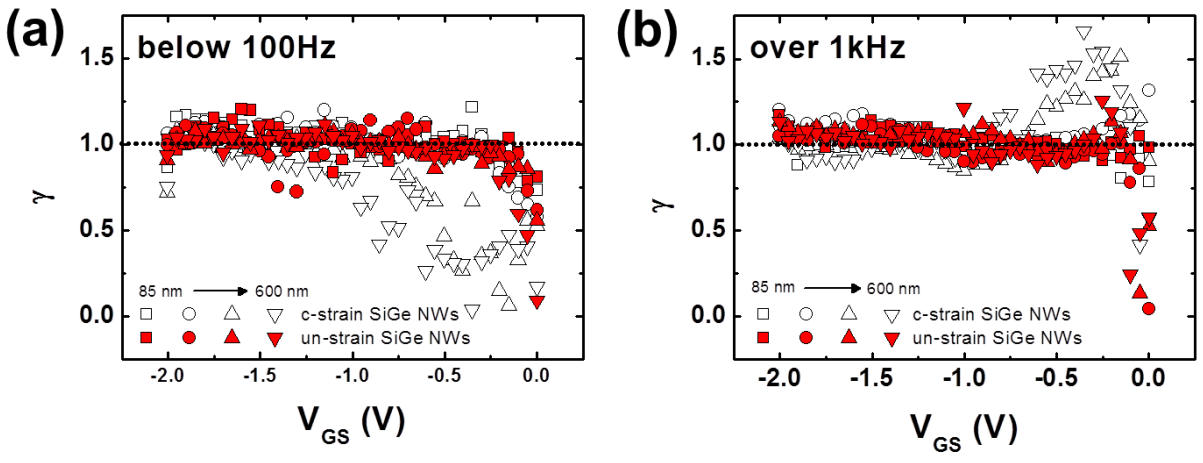


Figure 5.12 Distribution of γ as a function of the gate voltage (a) below 100 Hz and (b) over 1 kHz.

5.2.3.4 Influence of strain effect on the LF noise

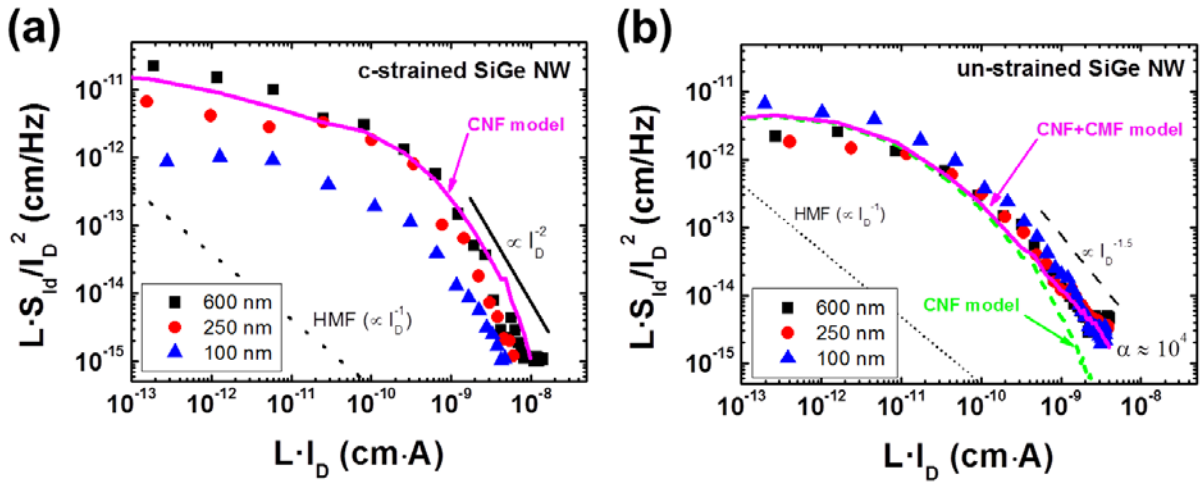


Figure 5.13 Drain current noise power spectrum normalized by the drain current and the channel length of (a) c-strained SiGe NWs and (b) un-strained SiGe NWs for V_{DS}=50 mV and f=20 Hz. Solid lines (pink color) are fitting curves for 600 nm channel length devices.

To decide whether the HMF or the CNF is the more appropriate model for interpreting the LF noise results, it was worth plotting the normalized drain current noise S_{Id}/I_D^2 as a function of the drain current in log-log scale as discussed in chapter 3. As it is shown in Figure 5.13, the overall pattern of normalized drain current noise varied according to the g_m/I_D^2 characteristic of the transistor and not as the reciprocal of the drain current ($1/I_D$). This clearly suggests that the LF noise in c-strained and un-strained SiGe nanowire FETs does basically stem from CNF model and not from HMF model. Interestingly, un-strained SiGe nanowire FETs are well-fitted together with the correlated mobility fluctuation (CMF) model is considered whereas the c-strained SiGe devices is enough with normal CNF model. It should also be noted that, at high drain current, the normalized current noise decreases less drastically than g_m/I_D^2 due to the presence of additional correlated mobility fluctuations. It means that there is some different effect for the influence of trapped charge in the channel between c-strained and un-strained devices.

Based on CNF model, the volume trap density N_t ($cm^{-3}eV^{-1}$) can be extracted from the flat-band voltage fluctuations S_{Vfb} as

$$S_{Vfb} = \frac{q^2 kT\lambda N_t}{fWLC_{OX}^2} \tag{5.4}$$

where q is the electric charge, k the Boltzmann constant, T the absolute temperature, λ the

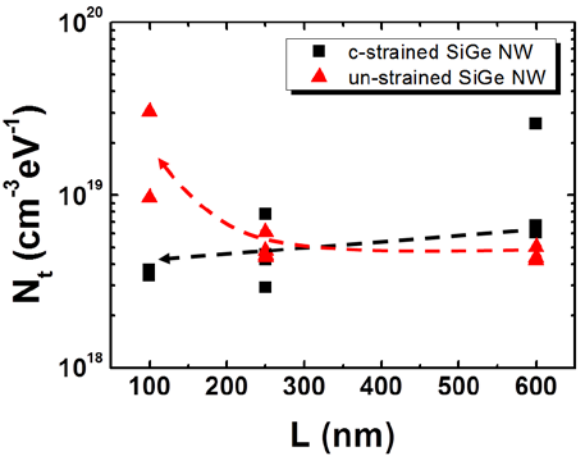


Figure 5.14 Extracted volume trap density N_t as a function of channel length.

oxide tunneling distance, f the frequency, W the channel width, and L the channel length. The extracted N_t are in the range of 2.9×10^{18} to 4.3×10^{19} cm^{-3}eV^{-1} for both devices. The tunneling distance λ was used 1.4×10^{-8} cm for the Si/HfO_2 system [200] in spite of the existence of Si capping layer at the interface. The extracted values of N_t are comparable to those obtained in high-k MOS planar devices [152], both of which are 10 to 50 times larger than in bulk silicon MOSFETs with SiO_2 gate oxide. As shown in Figure 5.14, in the case of the un-strained SiGe NWs, N_t is three to four times larger in short channel than in long devices, whereas for c-strained SiGe NWs, it is slightly reduced. This difference between un-strained and c-strained NWs could be attributed to retarded boron diffusion in c-strained devices that could induce different defect profile near S/D junctions for un-strained ones [201], [202].

To confirm the influence of correlated mobility fluctuations, the Coulomb scattering coefficient α_C associated to the CNF+CMF model have been extracted specifically by plotting the squared root of the normalized input gate voltage noise given by [174],

$$\sqrt{\frac{S_{Vg}}{S_{Vfb}}} = 1 + \alpha_C \cdot C_{OX} \cdot \mu_{eff} \cdot \frac{I_D}{g_m} \tag{5.5}$$

where S_{Vg} is the input gate voltage noise obtained by $S_{Id}/g_m{}^2$. Figure 5.15 (a) shows the estimation of α_C verified experimentally by Equation 5.5, allowing to be extracted from the slope of the observed straight lines. In Figure 5.15 (b), the extracted values of α_C are distributed as a function of gate length. For un-strained SiGe NWs, is roughly over 4×10^4 Vs/C, whereas, for c-strained SiGe NWs, is typically around 4×10^3 Vs/C, indicating that the CMF are significantly reduced in c-strained NWs. This feature could likely be attributed to the fact that, for c-strained channels, there is a better carrier confinement in the SiGe core-shell than in the un-strained ones. Indeed, for 20% Ge content, an additional 100 meV strain-induced valence band offset is expected [187]. As a result, un-strained devices present more surface mode operation than c-strained ones, rendering more efficient the remote Coulomb scattering from oxide/Si cap interface charges and thereby increasing the coefficient in CMF process. According to the remote Coulomb scattering theory [203], a reduction in one decade

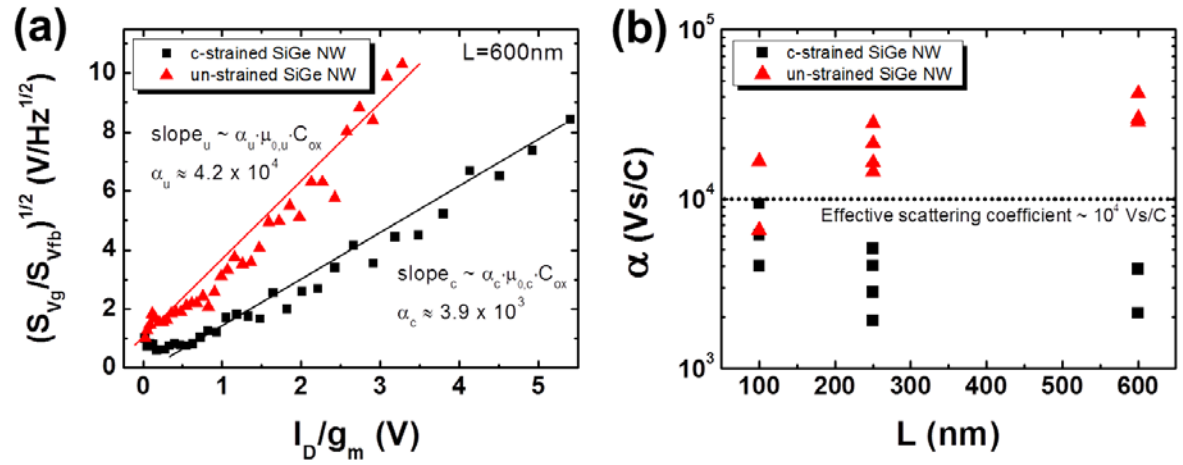


Figure 5.15 (a) Normalized input gate voltage noise ($\sqrt{S_{Vg}/S_{Vfb}}$) at 600 nm length and (b) extracted Coulomb scattering coefficient α_c as a function of channel length.

of corresponds to about 1.7 nm additional remoteness for c-strained NWs, which is in agreement with the effect of silicon cap around 1 ~ 1.5 nm.

In order to confirm this analysis, we have examined the mobility behavior for c-strained and un-strained devices in strong inversion region where surface roughness scattering prevails. To this end, the effective mobility was evaluated from the I_D-V_{GS} characteristics at strong inversion using the following standard approximation:

$$\mu_{eff} = \frac{I_D L}{WC_{OX}(V_{GS} - V_{TH})V_{DS}} \tag{5.6}$$

Then, the surface roughness limited mobility component μ_{SR} was deduced from the slope of the derivative of the reciprocal effective mobility at high gate voltage drive as [204]

$$D_{eff} = \frac{d(1/\mu_{eff})}{dV_{GS}} = \frac{\theta_1 + 2\theta_2(V_{GS} - V_{TH})}{\mu_0} \tag{5.7}$$

In Figure 5.16, the extracted surface roughness limited mobility are plotted as a function of channel length at V_{GS} = -2 V. It appears that the un-strained SiGe NWs show three times smaller surface roughness limited mobility than c-strained SiGe NWs, revealing that the surface roughness scattering is much larger in un-strained NWs, which is likely due to the enhanced carrier confinement closer to the oxide/Si cap interface. This is consistent with the conclusion drawn from the CNF+CMF noise analysis showing an attenuation of the Coulomb scattering coefficient for c-strained NWs.

In summary, LF noise was compared in c-strained and un-strained SiGe core-shell NW p-MOS devices. We found that, in both devices, LF noise can be well interpreted by the

CNF+CMF model. The un-strained SiGe NWs showed much larger Coulomb scattering coefficient and much lower surface roughness limited mobility. These features clearly indicate that the un-strained NWs operate more on the surface than the c-strained devices do, which makes the un-strained devices more susceptible to the Coulomb and surface roughness scatterings. In contrast, the c-strained NWs fully benefit from the core-shell architecture, which allows the carriers to remain more confined farther from the oxide/Si cap interface.

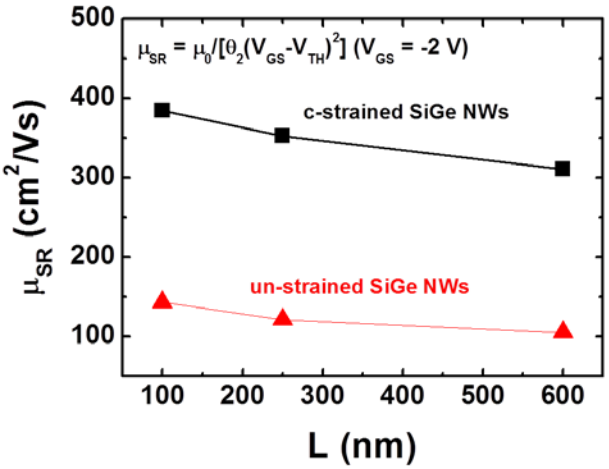


Figure 5.16 Surface roughness limited mobility (μ_{SR}) as a function of the channel length.

5.2.3.5 RTS noise analysis in gate leakage current

In long-channel (600 nm) c-strained SiGe NW FETs, the random telegraph signal (RTS) noise from the gate leakage current was partially observed depending on samples. It was obviously shown in off-state of a device at low drain voltage. Figure 5.17 (a) exhibits the variation of S_{Id} as changing from 0 V to 0.5 V in the gate voltage. At V_{GS}=0.5 V, the noise spectrum is similar to Lorentzian with $1/f^2$ behavior. In this region, such noise spectra should be not appeared because the device is fully turned off (i.e. no current). But the noise is caused by the gate leakage current. To confirm the RTS noise displayed as discrete switching events in the time domain, the gate leakage current was measured for ~ 20 seconds as shown in

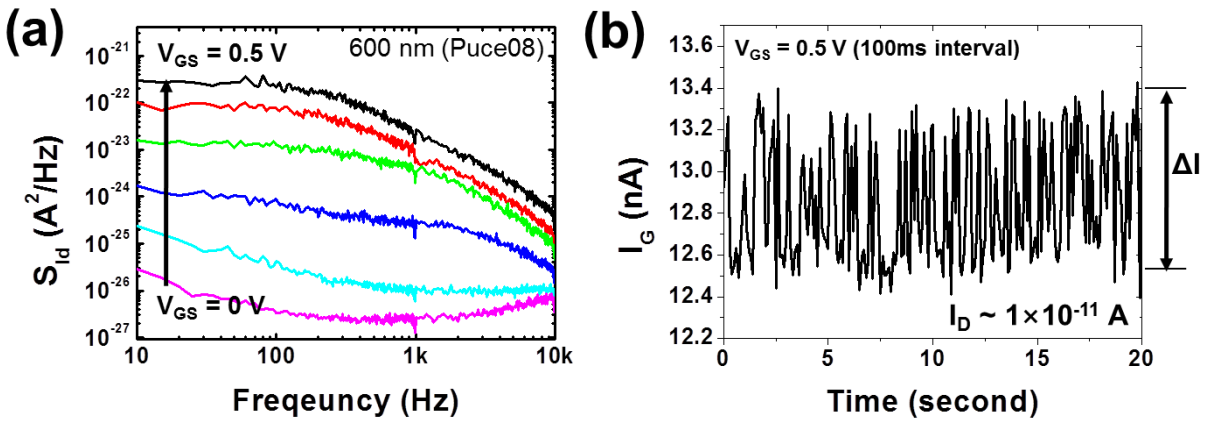


Figure 5.17 (a) Noise spectrum from the gate leakage current and (b) typical time domain plot of the gate current for RTS noise.

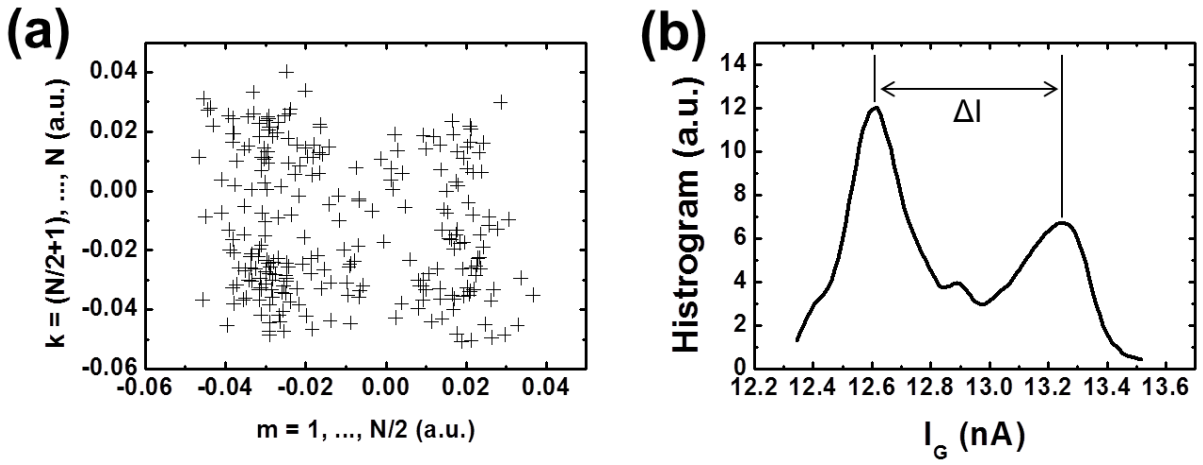


Figure 5.18 (a) Noise distribution by the noise scattering pattern (NSP) method and (b) histogram of current amplitude in time domain.

Figure 5.17 (b). The behavior is somehow close to the RTS noise but it is not obvious.

For clear understanding of RTS noise, the noise scattering pattern (NSP) method [205] and histogram of the current amplitude [113] were used. For the NSP method, the sequence of time domain data z[n] (n=1, 2, ... N) is plotted with two subsequences x[i] (i=1, 2, ... N/2) and y[j] (j=(N/2)+1, ... N) as shown in Figure 5.18 (a). The noise pattern with two subsequences exhibits the two-level RTS noise. Similarly, Figure 5.18 (b) shows the two-level RTS noise with the histogram of the gate current amplitudes and the histogram provides the average gate current RTS amplitude ΔI_G. The gate leakage current spectral density of a RTS exhibits a Lorentzian spectrum

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_l + \tau_h)[(1/\tau_l + 1/\tau_h)^2 + (2\pi f)^2]} \tag{5.8}$$

where τ_l and τ_h are the transition time for the low (or capture) and high (or emission) level, respectively. The fitting results of RTS noise with two-level traps were illustrated in Figure 5.19. The time constant property of two different trap components in the oxide for long-channel c-strained SiGe NWs was estimated. For the first trap, its transition times for the low and high level are same value of 1 ms and the other trap has 0.09 ms and 0.9 ms, respectively.

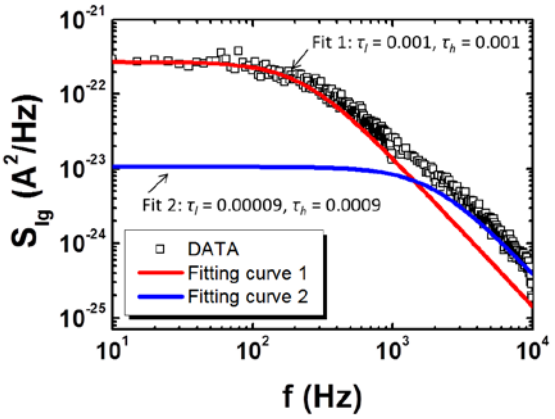


Figure 5.19 Curve fitting of RTS noise in the gate leakage current.

5.2.4 Noise comparison between Si and SiGe nanowire *n*-type FETs

Next, the noise level was compared mainly in the *n*-type Si nanowire FETs also with a c-strained SiGe device and a fully-depleted SOI (FD-SOI) FET according to the channel strain or H_2 annealing process. The detailed specifications for the comparison are summarized in Table 5.1. As shown in Figure 5.4, the cross-sectional TEM image of normal Si nanowire shows a rectangular structure (Figure 5.4 (b)) while H_2 annealed Si nanowire has a circular cross-sectional TEM image (Figure 5.4 (c)). In 2009, K. Tachi et al. [194] reported that the electron mobility of the rectangular Si nanowire FET is degraded as decreasing the channel width of nanowire on account of the impact of the lower electron mobility on (110) sidewalls. On the other hand, in circular shaped Si nanowire (annealed by H_2), the mobility is clearly degraded compared to the rectangular one. It is due to the mobility degradation at low inversion charge density. For both devices, the mobility at high inversion charge density is degraded compared to the FD-SOI FET owing to the higher surface roughness effect. However, the circular nanowire improves the mobility at high inversion charge region by reducing the surface roughness with H_2 annealing.

As shown in Figure 5.20, typical I_D-V_{GS} characteristics and the transconductances g_m for all devices are measured experimentally. On the whole, the FD-SOI FET shows the best device characteristics. The Si nanowires (rectangular) have the better performances compared to other nanowires and the H_2 annealed Si nanowires (circular) shows weird curve. It might be due to metal contact damage after the annealing process because the metal contact electrodes were dirty with the microscopic images. To confirm the differences of noise for Si and SiGe nanowires, the noise measurements were performed in the same way. The nanowire

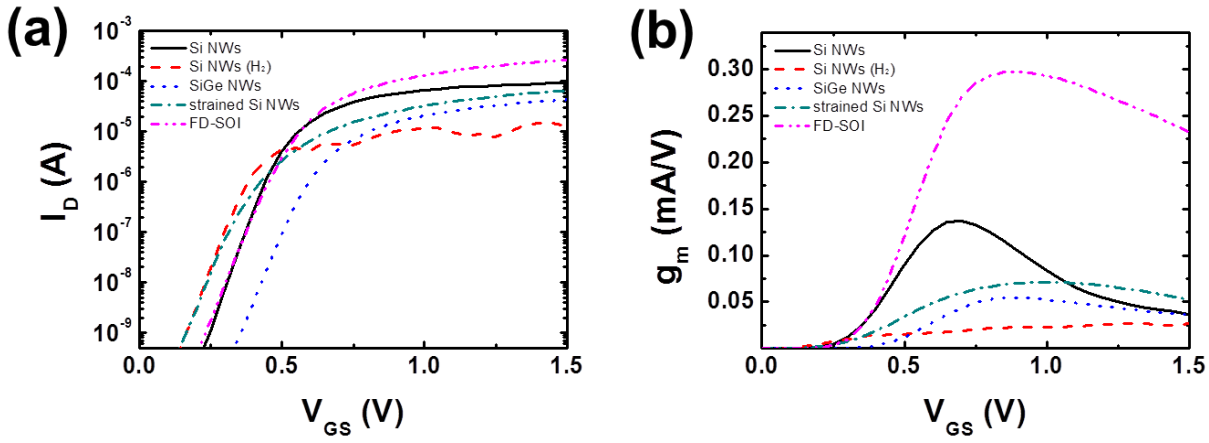


Figure 5.20 Drain current (I_D) and transconductance (g_m) curves as a function of the gate voltage between Si (rectangular), H_2 annealed Si (circular), SiGe, c-strained Si nanowires and FD-SOI FETs.

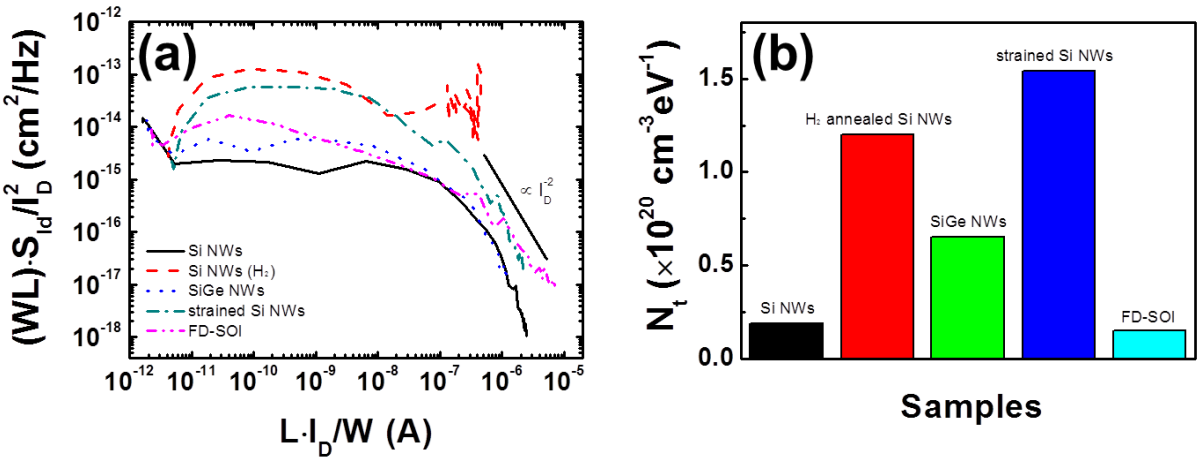


Figure 5.21 (a) Normalized LF noise power spectrum for Si and SiGe nanowires FETs depending on the channel strain and H2 annealing process. And c-strained SiGe nanowire and FD-SOI FET are also compared. (b) Comparison of extracted volume trap densities.

channel width was measured by TEM images. Because the total channel width and length of devices are different depending on samples, the normalized drain current noise (S_{Id}/I_D^2) is normalized again with the channel width and length. And the drain current also normalized with the channel width and length.

Hence, the results are shown in Figure 5.21 (a). The noise level in H_2 annealed (circular) and strained Si nanowires are much higher than other devices and Si nanowire (rectangular) reveals lowest noise. In detail, extracted volume trap densities N_t are compared and summarized in Figure 5.21 (b). The N_t for SiGe nanowire is about 3 times higher than for normal Si nanowires and other treatment such as channel strain or H_2 annealing for Si nanowires cause huge traps in the oxide or at the interface.

Table 5.1 Device specifications of *n*-type Si and SiGe nanowire FETs.

Structure	L_{eff} (nm)	W_{total} (μm)	C_{OX} (F/cm^2)	Sample N°
Si NWs	290	11.80	2.58×10^{-6}	K905(P03)
Si NWs (H_2 annealing)	290	9.08	2.03×10^{-6}	K901(P08)
strained Si NWs	290	9.89	1.55×10^{-6}	K905(P15)
SiGe NWs	290	12.01	2.31×10^{-6}	K905(P06)
FD-FET	250	10.00	2.00×10^{-6}	J340(P04)

5.3 Nanotubes and nanowires based on Bottom-up approach

In the section “Nanotubes and nanowires based on Bottom-up approach”, the electrical properties and LF noise in junctions such as metal-semiconductor junctions in the carbon nanotube and GaN nanowire devices will be presented. The devices were fabricated based on the Bottom-up technology with colleagues in KRISS (Korea Research Institute of Standard and Science), Yonsei University, and KIST (Korea Institute of Science and Technology). In here, we will show that the noise characterization can be a valuable tool to decide good contacts in fabricating nano scale devices together with the importance of junctions.

5.3.1 Metal-semiconductor junctions in multi-walled carbon nanotubes

Since discovery of carbon nanotubes (CNTs) [10], nanotube devices have been attracted great attention to supplement the conventional CMOS technology. However, the reliability and reproducibility of nanotube devices hinder systematic study. Even though many studies for nanotube devices have been continued, the different experimental results despite of same kind of devices are embarrassed for the applications. This implies a delicate change of the electrical properties in nanotube devices by the metal-nanotube contacts, tube-tube junctions, defects in the narrow channel, or various geometric shapes [206-208]. Moreover, a large 1/f noise in CNTs has been reported in individual or network structures and the origins of the noise were attributed to small defects in narrow channels, ambient gas adsorption/desorption conditions and charge traps in the oxide layer [32-34], [209], [210]. In here, LF noise in individual multi-walled carbon nanotubes (MWNTs) was investigated with different metal electrodes. As the electrical transport of nanotube devices gets closer to quasi-ballistic transport, the noise becomes more sensitive to the resistance of the devices. This means that there is a significant influence of the electrical contacts on the electrical noise, suggesting the importance of a criterion for deciding good contacts in fabricating nanotube devices.

Devices were fabricated on the silicon oxide substrate in a two-probe configuration with different metal electrodes using MWNTs (Sigma-Aldrich), of which the diameter is ~25 nm (see reference [211] for details). A simple selective electron beam technique was used to form the individual contact on MWNTs [26]. For the metal contact, Ti/Au, Cr/Au, Pd/Au, and Pt/Au (20/50 nm), were deposited by e-gun evaporation. To make better metal contact, a rapid thermal annealing (RTA) process was performed at 300 °C during 30 seconds. Each

work-function of different metals is summarized in Table 5.2. The work-functions of multi- and single-walled carbon nanotubes have been known to be 4.95 and 5.05 eV, respectively [212]. The difference of work-function with Ti or Cr metals is larger than with Pd or Pt so that Ti- or Cr-contacted nanotube devices will be significantly influenced by the formation of the shallow Schottky barriers.

Table 5.2 Work-function of metals

Metal	Work-function
Ti	4.33 eV
Cr	4.5 eV
Pd	5.22 ~ 5.6 eV
Pt	5.12 ~ 5.93 eV

The static and noise measurements were performed in a dark box and ambient gas conditions at room temperature. Most devices show linear *I-V* characteristics by two-probe measurement including the contact resistance of the electrode metals, reflecting the validity of the comparison of the *I-V* characteristics even in a two-probe configuration. Specifically, representative *I-V* characteristics of MWNT devices with different metal contacts are plotted as shown in Figure 5.22. For the sample A (Pd), B (Cr), and C (Ti) exhibit an Ohmic behavior different from the sample D (Ti). The resistances of sample A, B and C were expressed as $1.0R_0$, $2.0R_0$ and $23.6R_0$, respectively, where R_0 is the quantum resistance given by the relation of $R_0=h/2q^2=12.9$ kΩ, which can be a criterion for a ballistic conductor or a diffusive conductor. Considering the small resistance of sample A, of the order of a quantum resistance, the Pd contacted device (sample A) may be ballistic, but we regarded it as quasi-ballistic owing to the possibility of several conduction paths in MWNTs. On the other hand, the Cr or Ti contacts show characteristics of diffusive transports, which have bigger resistance than the quantum resistance.

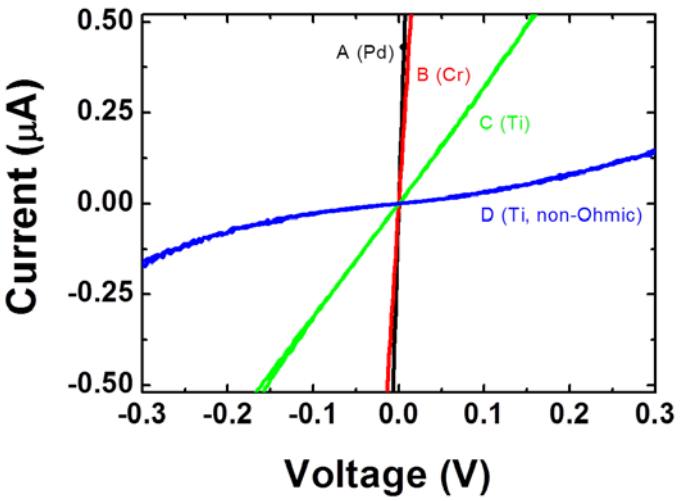


Figure 5.22 *I-V* characteristics of individual multi-walled nanotube devices with different metal contacts at room temperature.

The electrical noise of MWNTs was measured as a function of the frequency, ranging from 10 Hz to 1 kHz, at different current levels. Between two difference noise models, the Hooge mobility fluctuation (HMF) model is known to be appropriate for condensed materials like metal and bulk semiconductors. For an intuitive comparison, the current noise of MWNT

devices was analyzed with the HMF model,

$$\frac{S_I}{I^\beta} = \frac{\alpha_H}{Nf^\gamma} \tag{5.9}$$

where α_H is the Hooge parameter depending on the defect condition of the materials, N the total number of carriers in the channel, and β, γ are the scaling exponents with the current and the frequency respectively. The frequency exponent γ was calculated to be 1.06±0.1 including the non-Ohmic devices (sample D) and the current exponent β of Ohmic samples (A, B, and C) were estimated to be about 2 whereas the sample D was 1.56. Irrespective of the kind of metals, smaller β was observed in every sample with the non-Ohmic characteristics. This can be explained by the component of the diode noise characteristics with the exponential dependence originating from the formation of Schottky contacts with lower work-function than that of carbon nanotubes [213].

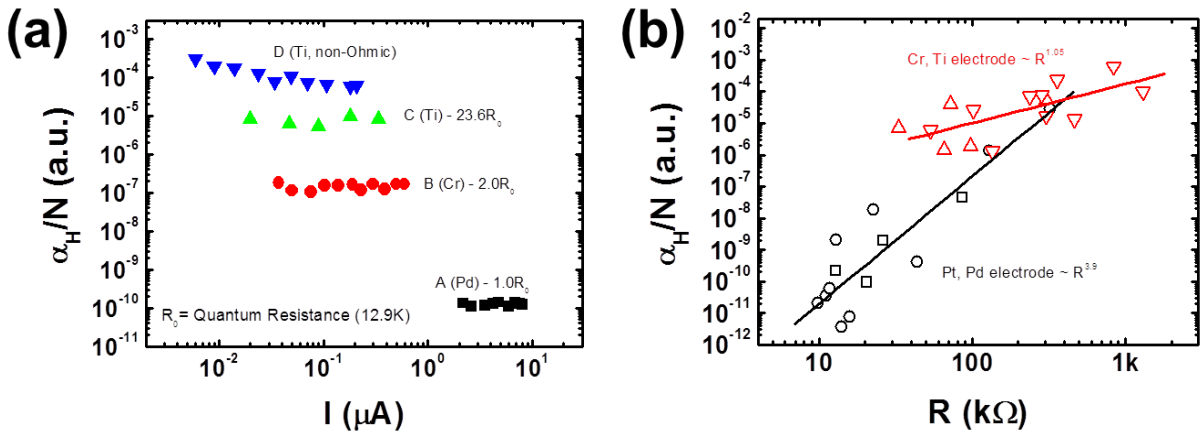


Figure 5.23 Noise amplitude as a function of (a) the current and (b) the resistance of individual MWNTs with different metal electrodes.

In Figure 5.23 (a), the noise amplitude α_H/N was used for the comparison between different metal contacts because it was difficult to estimate the total carrier number N in MWNTs. The noise amplitude of Ohmic contacts was constant owing to no gate dependence of the metallic MWNTs. In the case of the sample D, there is a slight slope with the increase of the current, which is attributed to the different current dependence for the noise. The Pd contacted devices having a quasi-ballistic conductance exhibits the lowest noise amplitude, 10^{-10}, but Cr or Ti contacts appears quite high noise amplitudes, 10^{-7} or 10^{-5}, which are in the range of the previous reports [214]. In the comparison between the Pd-contacted and Cr-contacted MWNTs, the difference of the resistance was only twofold, but the noise of the Cr-

contacted MWNT was surprisingly 1000 times larger than the Pd-contacted one, as shown in Figure 5.23 (a). The remarkable difference can be noticed in Figure 5.23 (b), which shows the noise amplitude as a function of the resistance of MWNT with different metal electrodes. For the devices with Cr and Ti contacts, the noise amplitude follows $10^{-10.2}R^{1.05}$, in agreement with previous report [32]. Considering the noise source of the network comes from the inter-connection between the nanotubes, the contact property between MWNTs and the metal electrodes can mainly affect the noise patterns, in the case of Cr and Ti electrodes. However, for Pd and Pt contacts, the noise falls rapidly with the decrease of the resistance, following $10^{-26.3}R^{3.9}$. The large exponent, 3.9, is similar to the exponents Q of 2-D metal films, Q ($\equiv\partial(\log S_R)/\partial(\log R)$), ranging from 4 to 8 [215]. From Figure 5.23 (b), the Q value of MWNT devices with Pd and Pt electrodes was extracted to be 5.9, which is similar to the results in the thin metal film or the graphene treated by sandblasting and oxygen plasma [216]. Because the electrical contacts by Pd or Pt showed characteristics of quasi-ballistic conduction, the influence of contacts on the noise should be much smaller than the case of Cr or Ti, indicating the dominance of the channel part for the Pd or Pt cases [217]. Finally, it is confirmed that the noises of MWNTs with Pd and Pt electrodes reflect the influence of the channel with a high resistance exponent of the noise power spectrum, different from Ti and Cr electrodes with the extra contribution of the contact potentials resulting in the smaller exponent. The noise was clearly observed to have $1/f$ shape irrespective of the different metals or the Ohmic behavior.

5.3.2 Quality index for metal contacts – GaN nanowire

GaN nanowires have drawn much attention in the view point of nano-electronics and photonic devices. They exhibited good switching behaviors with very large conductance swings and rectifying electrical properties for devices and logic circuits [218-220]. In addition, they can be used as a light source having various wavelengths in photonic system [221]. However, like all other nanowire structures, the metal-semiconductor contacts play an important role for the limitation of the device performances. Depending on the device applications like a diode or a transistor, for example, the linear or non-linear electrical behaviors have been demanded with the metal contact. The appropriate metallization can be achieved using the work-function calculation between metal and nanowire but cannot be controlled its quality during the process. In particular, it is hard to quantitatively determine the quality of metal-semiconductor contact using the conventional DC measurement. Since it

has been known that the metal contacts also affect the noise, herein the quality of metal contact on the GaN nanowire was investigated using the low-frequency noise measurement [211].

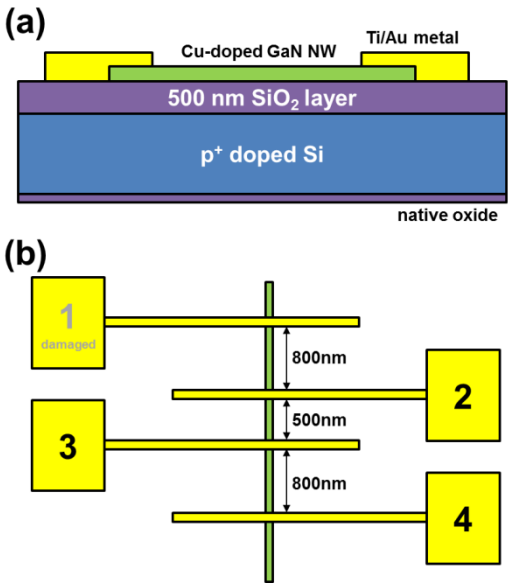


Figure 5.24 GaN device: (a) schematic and (b) top-view images

The GaN device was fabricated on the p^+ doped Si substrate having 500 nm SiO_2 film by co-workers at Yonsei University and KIST. Sub 100 nm Cu-doped GaN nanowire was used and it was expected to be heavily doped by *n*-type. It was confirmed that there is no gate dependence in spite of thick oxide layer (not shown in here). For metallization, Ti and Au were deposited with thickness of 10 and 80 nm, respectively. Figure 5.24 shows the device schematic and top-view images of GaN device.

At the first, the GaN device had a four-probe configuration but one metal contact was broken during the measurement. For this reason, the *I-V* measurement was performed between other three electrodes. As shown in Figure 5.25 (a), they exhibits nearly linear (Ohmic) behaviors in *I-V* characteristic and the length dependence is also observed. Since the Cu-doped GaN nanowire is heavily doped, the Ohmic behavior is predicted. For each channel length between the metal electrodes, the conductance and resistance is summarized in the inset of Figure 5.25 (a). To confirm the linearity of conductance strictly, the current is differentiated with the voltage. As shown in 5.25 (b), it appears some weak non-linear properties depending on the electrodes. It might be due to a weak Schottky barrier of the metal/nanowire junction or poor

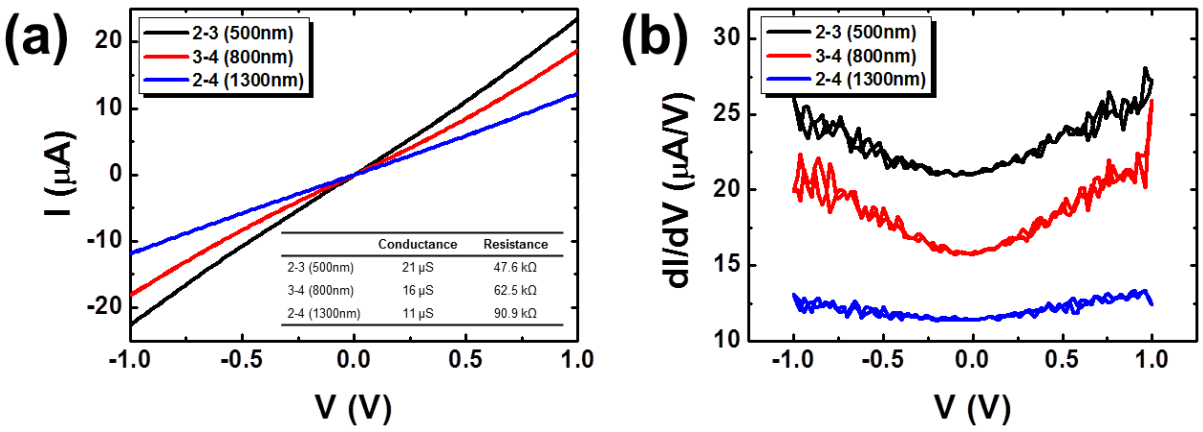


Figure 5.25 (a) *I-V* characteristics of each electrodes having different channel length in a two-probe configuration. (b) Differentiated conductance as a function of the voltage.

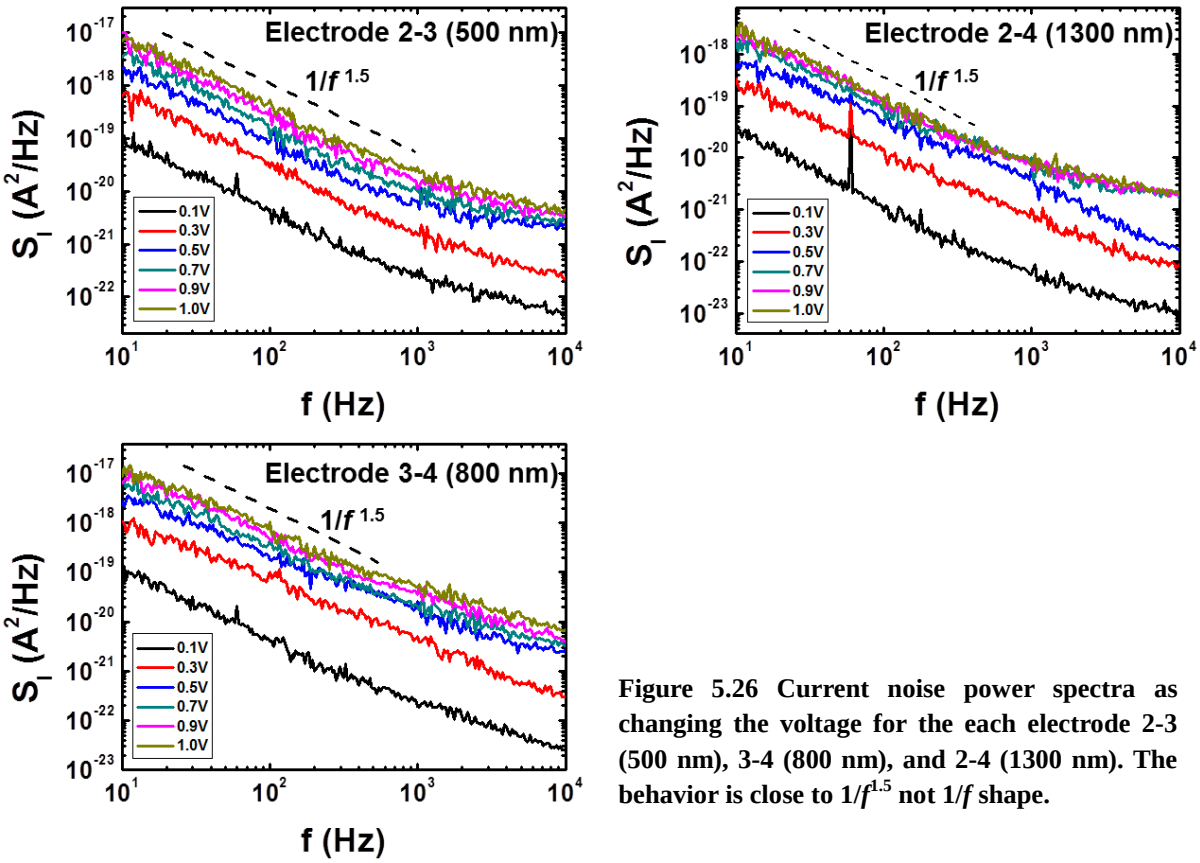


Figure 5.26 Current noise power spectra as changing the voltage for the each electrode 2-3 (500 nm), 3-4 (800 nm), and 2-4 (1300 nm). The behavior is close to $1/f^{1.5}$ not $1/f$ shape.

contact quality.

The current noise power spectrum (S_I) for each electrode was measured as changing the voltage as shown in Figure 5.26. At lower voltage, the slope of S_I is proportional to $1/f^{1.34\sim1.39}$ but it has become slow about $1/f^{1.21\sim1.23}$ as increasing the voltage. These values are similar to the previous report for GaN nanowires [222]. And the noise is also proportional to I^2. In this device, it cannot be proper with CNF model because the nanowire is heavily doped and there is no interaction between the channel and the oxide layer. Before the comparison of noise level between electrodes, the noise and current should be normalized. For the current relation with the channel length is

$$I = \frac{V}{R} = \frac{A}{\rho L}V \tag{5.10}$$

where ρ is the resistivity and A is the channel area. For the S_I, the total carrier number N is estimated with $n=L/q\mu AR$ as

$$N = \frac{L^2}{q\mu R} \tag{5.11}$$

Therefore, the current normalized noise is

$$\frac{S_I}{I^2} = \frac{\alpha_H}{Nf^\gamma} = \frac{\alpha_H Rq\mu}{L^2 f^\gamma} = \frac{\alpha_H q^2 \mu^2 n}{LAf^\gamma} \tag{5.12}$$

In Figure 5.27 (a), the normalized current is compared considering the different channel length. The noise for the electrode 2-3 is much lower than the others but the electrodes 3-4 and 2-4 are similar together. It means that the total noise of 2-4 might be mainly limited by the electrode 4 since the noise in electrode 2-3 is lower than 2-4. It is thought that the electrode 4 has poor quality compared to the others. The origin of different noise level for the poor contact was observed with an atomic force microscopy (AFM) as shown in Figure 5.27 (b). The broken nanowire between the electrode 1 and 2 can be confirmed. In the case of electrode 4, the metal made a contact formation at the end of nanowire. In general, the synthesized nanowire has a particle such as a catalyst on either end of nanowire. This particle may be affected the contact quality. The result shows that low-frequency noise measurement technique can be a tool to access the quality of metal contact for the nano devices even if there are some works to find the clear understanding the mechanism.

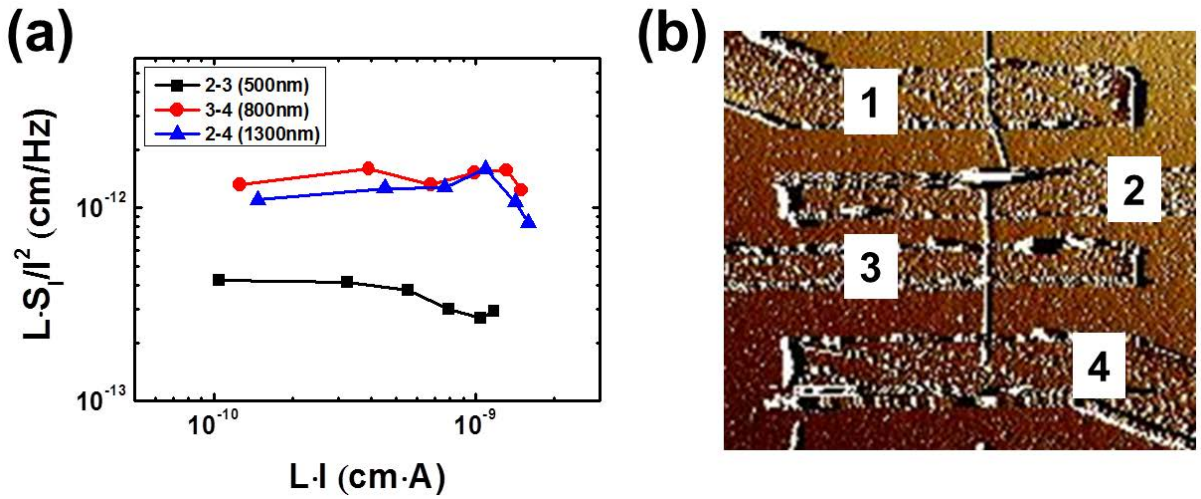


Figure 5.27 (a) Normalized noise comparison between different electrodes. (b) AFM image of Cu-doped GaN device.

5.4 Summary: Impact of channel strain and metal contact

Nanowire and nanotube structures are representative materials for the nano technology due to their interesting physical and electrical properties. However, there are also some limits for the reproducibility, the control, and the device performance because of the smaller size which is defined at least between 1 and 100 nm. To overcome these issues, the study of the nanowires and nanotubes has been performed from the perspective of both sides between the top-down and bottom-up approaches.

Si and SiGe nanowires by top-down fabrication process are interesting for the GAA structured MOS devices providing better gate control. In addition, the 3-D stacked structure and the channel strain technique compensate the small output current of nanowires due to its size. For other nanowires or nanotubes fabricated by the bottom-up process, the metal-semiconductor junction is also important because the junction induces the energy barrier such as Schottky barrier. In the chapter 5, the impact of channel strain and metal-semiconductor junction for nanowires and nanotubes was studied based on the LF noise analysis. For the LF noise between c-strained and un-strained SiGe *p*-type FETs, it is mainly originated from the carrier number fluctuations and their volume trap densities are similar. However, the un-strained SiGe devices appear larger influence of correlated mobility fluctuations coming from the trapped charge carriers and it is due to the channel strain. The result indicates that the c-strained SiGe devices have some advantages for the current boost and the LF noise reduction even if the noise level mostly depends on the oxide traps. The LF noise also is changed depending on materials and annealing processes. From the studies of metal-semiconductor junctions with nanowires and nanotubes, it shows that the LF noise is affected by the Schottky barrier and it can be a useful to determine the quality of metal contact.

Chapter 6 Graphene

6.1 Physical Backgrounds

6.1.1 Electronic structure and carrier transport

Since the successful separation of a single layer graphene from graphite using a simple mechanical exfoliation technique in 2004 [12], it arose enormous interests and fervent activities on graphene research. The graphene is a 2-D material containing carbon atoms tightly bonded together in a honeycomb lattice. Unlike a conventional 2-D system that is formed at the buried semiconductor interfaces like a two-dimensional electron gas (2DEG), the graphene is an ideal 2-D system. It is due to the non-interacting π and π* states by carbon atoms in single atom thickness. The unique band structure was firstly estimated by P. R. Wallace in 1947 [223]. The graphene consists of π-states from the valence band and π* states for the conduction band and these two bands touch at six points which called Dirac point (E_{Dirac}) or neutral point as shown in Figure 6.1 (b) [224]. It notes that these bands touch at E_{Dirac} indicates a zero band-gap in graphene. For this reason, it is generally accepted a zero-gap semiconductor or a semi-metal. The band structure of graphene having a linear dispersion is symmetric so that electrons and holes in ideal graphene (pure and free-standing) should have the same properties (Figure 6.1 (c)). The linear dispersion is reminiscent of the dispersion of light

$$E = c\hbar k \tag{6.1}$$

where c is the light velocity. In addition, there are two sub-lattices, A and B (Figure 6.1 (a)), in the structure of graphene allows the Hamiltonian describing it to be written in the form of a relativistic Dirac Hamiltonian

$$H = v_F \boldsymbol{\sigma} \cdot \hbar \mathbf{k} \tag{6.2}$$

where $\boldsymbol{\sigma}$ is a spinor-like wave function, v_F the Fermi velocity of graphene, and $\mathbf{k}$ the wave vector of the electron. Since there are two atoms in the unit cell of graphene, it causes the spinor character of the graphene wave function (not from spin) [225].

The electrons of graphene can be described as relativistic particles which is given by

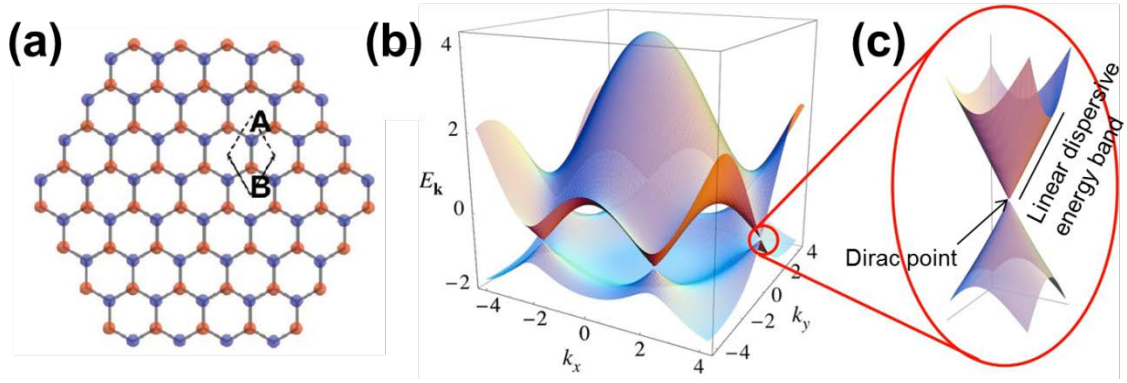


Figure 6.1 Hexagonal honeycomb lattice of graphene with two atoms (A and B) per unit cell. (b) 3-D electronic dispersion in the honeycomb lattice of graphene. (c) Energy band close to one of the Dirac points.

$$E = \sqrt{m_p{}^2 c_p{}^4 + p_p{}^2 c_p{}^2} \tag{6.3}$$

where m_p is the rest mass, p_p the momentum, and c_p the velocity of the particle. In graphene, electrons behave as zero rest-mass, relativistic Dirac Fermions due to the linear dispersive energy bands. Therefore, Equation 6.3 can be expressed

$$E_{Graphene} = v_F p \tag{6.4}$$

These are major features to separate out compared to conventional semiconductors and it causes outstanding transport properties of graphene such as ballistic transport, quantum electrodynamics, chiral quantum Hall effects (QHE), minimum quantum conductivity, and so on [13]. For example, graphene exhibits an ambipolar transport such that charge carriers can be changed continuously between electrons and holes. The mobility can be up to 200,000 cm^2/Vs in the case of suspended, exfoliated graphene eliminating the interactions with the substrate [226], [227]. In ballistic regime, carriers move with a Fermi velocity of $v_F \approx 10^6$ m/s as expressed in Equation 6.4. Moreover, even at room temperature, the QHE can be observed in graphene. Another interesting point is that there is a zero-field conductivity close to the integer quantum conductivity experimentally ($=4q^2/h$) [228]. Particularly, these unique natures of charge carriers in graphene are well described with the Dirac equation rather than the Schrodinger equation that is a base in most condensed matter physics.

Nevertheless, these interesting electronic properties of graphene are mainly limited by scattering for applications. Indeed, the long channel graphene results in a diffusive transport by the elastic and inelastic collisions of carriers. The mechanisms for the elastic scattering are suggested as Coulomb scattering by charged impurities (primarily trapped charges in the substrate), short-range scatterers (e.g. defects), and surface roughness or ripples of the

graphene structure [224], [229], [230]. On the other hand, the inelastic scattering has been known to come from the phonons of graphene containing the surface phonons of a polar substrate [231], [232]. Hence, the mobility in single layer graphene typically decreased as increasing the carrier density due to the scattering [233]. For this reason, the mobility of graphene is reduced to 1,000 ~ 10,000 cm^2/Vs depending on the nature and purity of the substrate.

6.1.2 Research trends of graphene

As previously mentioned, graphene was first obtained by mechanical exfoliation method from graphite but this method provided only a small piece of graphene (i.e. a graphene flake) which is suitable for the fundamental study. In practice, it is slow and tough work to find a graphene flake after transfer process because the graphene flake is too thin and small on the substrate. Fortunately, graphene crystallites can be visualized on a certain thickness of SiO_2 (~ 300 nm) substrate using an optical microscopy [234]. Another difficulty is a geometrical shape of graphene with the method. Figure 6.2 shows various thicknesses of graphene and their geometric patterns. It is important to have appropriate shaped channel of graphene for the experimental purposes and it can be usually achieved by oxygen plasma [216]. However, for the large-area fabrication, graphene flake is as small as ever. Recently, there are several studies to synthesize graphene sheets for their cost, throughput, and size such as liquid-phase exfoliation, epitaxial growth by thermal desorption of Si atoms from the SiC surface, epitaxial growth by chemical vapor deposition (CVD) on transition metals, unzipping carbon nanotubes, and so on [235-239]. Among them, the CVD-based graphene is interesting for the

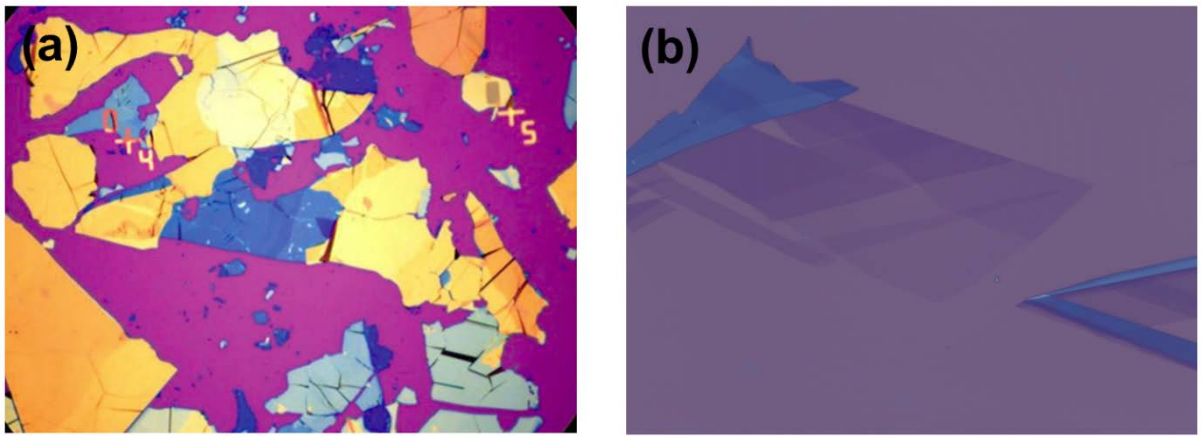


Figure 6.2 Graphene flakes on a surface of SiO_2/Si substrate. The different colors correspond to the thickness of graphene.

large-area fabrications.

Many studies of graphene are being in many fields such as electronics, chemical/bio sensors, transparent conducting films, optical devices, ultra capacitors, batteries, and etc. For high-frequency applications, graphene can be suggested. Indeed, Y. M. Lin et al. reported that the current gain and power gain in graphene transistors were achieved at frequencies as high as 100 GHz and below 14 GHz, respectively [240]. However, the existence of minimum conductivity leads to high leakage current in the off-state and it is limited for integrated circuits. For this, a band-gap engineering technique by quantum confinement or Coulomb blockade has been suggested to make low-dimensional graphene nanostructures such as graphene nanoribbons (GNR), quantum dots, and single electron transistors [241]. It is also mentioned for ultimately sensitive gas detectors [242] and ultrafast photo detectors [243]. In 2011, A. Vakil et al. noted that graphene can be metamaterials and transformation optics by designing and manipulating spatial patterns of graphene [244].

Despite of potential in graphene, its electrical and physical properties have not been understood clearly. There are many factors to dominate the properties such as scattering, flatness, edge effect, and domain size. Among them, the scattering is correlated to the noise properties. In the point of low-frequency (LF) noise, graphene which observed 1/*f* noise is also interesting. Beginning with a report for the suppression of 1/*f* noise in bilayer graphene devices by Y. M. Lin in 2008 [245], enormous studies have been achieved for three years as summarized in Table 6.1. They are much larger in a short period compared to other nano materials such as carbon nanotubes and nanowires and it proves their interests for the

Table 6.1 Low-frequency noise reports for graphene devices for 3 years (2008 – 2010).

Article	Authors	Journal (Year)
Strong Suppression of Electrical Noise in Bilayer Graphene Nano devices	Y. M. Lin et al	Nano Lett. (2008)
Low-frequency electronic noise in the double-gate single-layer graphene transistors	G. Liu et al	Appl. Phys. Lett. (2009)
Resistance Noise in Electrically Biased Bilayer Graphene	A. N. Pal et al	Phys. Rev. Lett. (2009)
Ultra noise field-effect transistors from multilayer graphene	A. N. Pal et al	Appl. Phys. Lett. (2009)
Electrical and noise characteristics of graphene field-effect transistors: ambient effects, noise sources and physical mechanisms	S. Rumyantsev et al	J. Phys. Condens. Matter (2010)
Enhanced Conductance Fluctuation by Quantum Confinement Effect in Graphene Nanoribbons	G. Xu et al	Nano Lett. (2010)
Effect of Spatial Charge Inhomogeneity on 1/f Noise Behavior in Graphene	G. Xu et al	Nano Lett. (2010)
Charge Noise in Graphene Transistors	I. Heller et al	Nano Lett. (2010)
Low-frequency noise and hysteresis in graphene field-effect transistors on oxide	S. A. Imam et al	Micro Nano Lett. (2010)

graphene. The noise study in graphene devices has been typically performed for the number of layers or device structures. The noise in single layer graphene devices decreases with increasing carrier density whereas bi and multilayer graphene devices behave oppositely by a suppression in noise by more than two orders [246]. In 2010, G. Xu et al. reported the inhomogeneous spatial charge effect on 1/*f* noise in graphene [247]. They reported that an M-shaped noise behavior was observed as changing the gate voltage in single layer graphene whereas bilayer graphene showed V-shaped noise behavior. On the other hand, I. Heller et al. suggested augmented charge noise model by J. Tersoff [29] considering fluctuations in close proximity of graphene sheet [248]. Since graphene is much sensitive to scattering effect in many reasons including a substrate, the LF noise study may help to understand the electrical and physical properties for graphene applications.

6.2 Device structure of graphene field effect transistors

In here, we will report the study of electrical and noise properties in graphene field-effect transistors (G-FETs) with single layer and bilayer graphene by the mechanical exfoliation and CVD growth method at Samsung Advanced Institute of Technology (SAIT).

The G-FETs with the mechanical exfoliation method was fabricated on a heavily p-doped Si substrate having 300 nm SiO_2 layer and Ti and Au metals were used for the electrode. In general, the number of graphene layer is confirmed with Raman spectroscopy [249]. In Raman spectrum, there are important peaks commonly which observed in graphene and graphite structure and they are called G (at 1580 cm^{-1}) and 2D (at 2700 cm^{-1}) peak as shown in Figure 6.3 (a). These peaks vary as changing the number of graphene layer (Figure 6.3 (b)). A G peak is increased as increasing the number of layer until a certain numbers and then it is

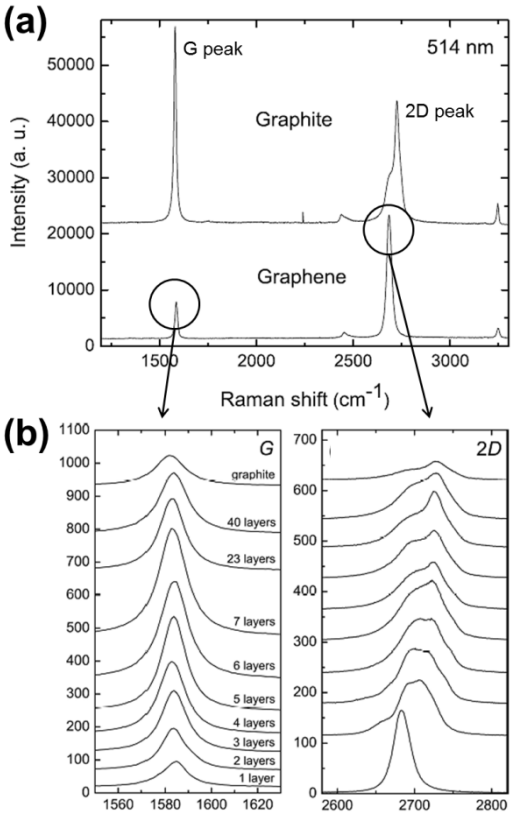


Figure 6.3 (a) Raman spectra for bulk graphite and graphene and (b) evolution of G and 2D band as functions of the number of graphene layers [249].

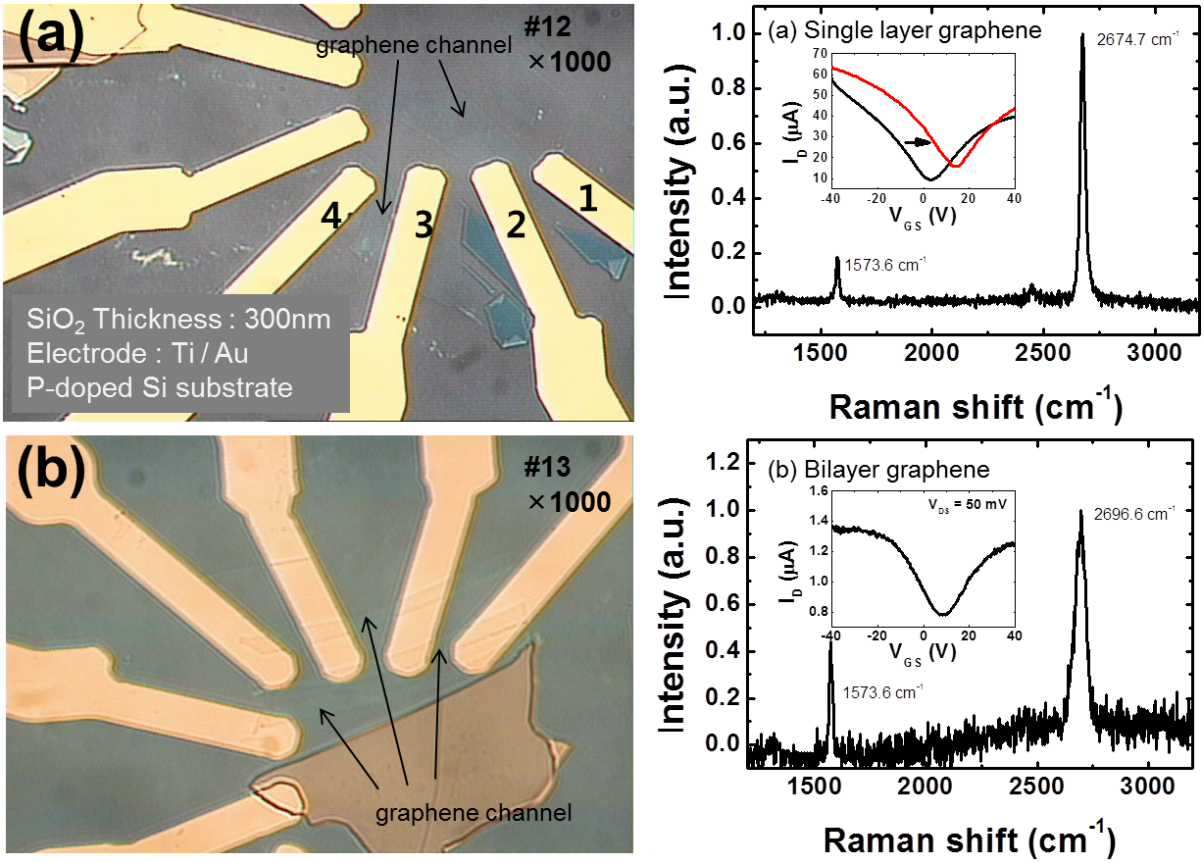


Figure 6.4 Optical images, Raman spectra (at SAIT), and I_D-V_{GS} characteristics of (a) single layer graphene and (b) bilayer graphene FETs.

decreased. In the 2D band, it shows a Lorentzian lineshape in single layer and narrow peak width whereas the shape is changed to mixture of several peaks as increasing layer. Figure 6.4 shows the optical images, Raman spectra, and I_D-V_{GS} characteristics of single and bilayer G-FETs using mechanical exfoliation method. As shown in figures, the channel has a geometric shape so that it cannot define the channel dimension. From I_D-V_{GS} characteristics, their ambipolar behavior and Dirac voltage (V_{Dirac}) were confirmed. At first, V_{Dirac} of single and bilayer graphene was estimated about 3.2 V and 8.3 V, respectively but it sometimes changed. It might be due to the revealed channel region for the ambient condition.

On the other hand, G-FETs with CVD grown graphene were also measured. The devices were fabricated in 6-inch wafer scale manufacturing process. The n^+-doped Si substrate with 100 nm thickness of SiO_2 layer was used for the bottom-gate electrode. The CVD graphene was put on the 6-inch wafer using transfer method. For the electrodes, 100 nm thickness of Au metal was deposited on the graphene without photo-resist (PR) coating process for preventing the influence of residual PR but the contact quality is not good. The various

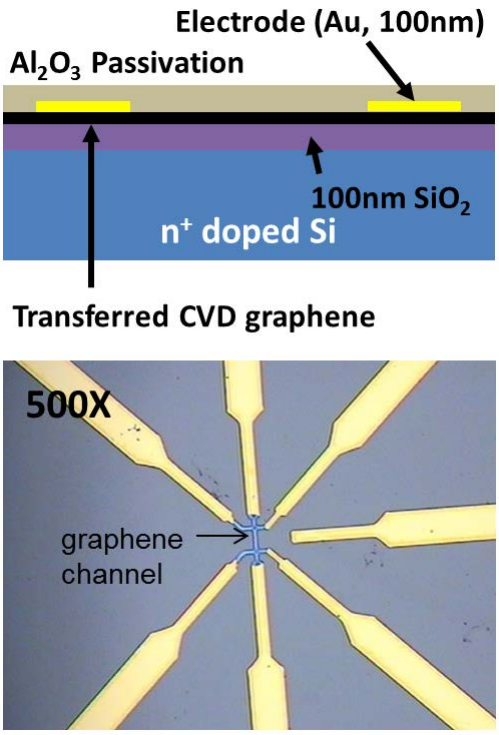


Figure 6.5 Schematic of a G-FET with CVD graphene and its optic image.

micro-scale channel widths and lengths were defined using plasma etching process. The channel regions including contacts were passivated with Al_2O_3 deposition. Figure 6.5 shows a device schematic and top-view optical image of G-FETs with CVD graphene.

The transfer characteristics were measured by a two-probe configuration measurement as changing the channel length and width. Depending on devices, V_{Dirac} is different despite of Al_2O_3 passivation. The length and width dependence are not clear due to the influence of large contact resistance. The results show that graphene is very sensitive to influence of surroundings. The detailed electrical and LF noise characterizations of G-FETs were performed with near 0 V of V_{Dirac}.

6.3 Electrical properties and low-frequency noise in G-FETs

6.3.1 Typical *I-V* characteristics & Length dependence

All measurements of G-FETs were performed in a metal box at room temperature. As shown in Figure 6.6, most of devices show the linear curves in I_D-V_{DS} characteristics with different gate voltage (Figure 6.6 (a)) and their ambipolar behaviors in I_D-V_{GS} characteristics are symmetric depending on the drain voltage (Figure 6.6 (b)). In I_D-V_{GS} characteristics, they exhibit an asymmetry between hole and electron conductions due to the pinning of the charge density at the graphene/metal interface [250-252]. In *n*-type conduction regime of G-FETs, a *p*-*n*-*p* structure forms along the graphene channel whereas a *p*-*n* junction in the *p*-type conduction regimes.

From Figure 6.6, the V_{Dirac} is estimated about 4 V and the minimum current (or maximum resistance) also exists about 0.35 μA. In general, the shift of V_{Dirac} has been well observed during the measurement of graphene devices originated by the adsorption of H_2O molecules on the substrate or on the graphene sheet [253]. Depending on the samples, there are some

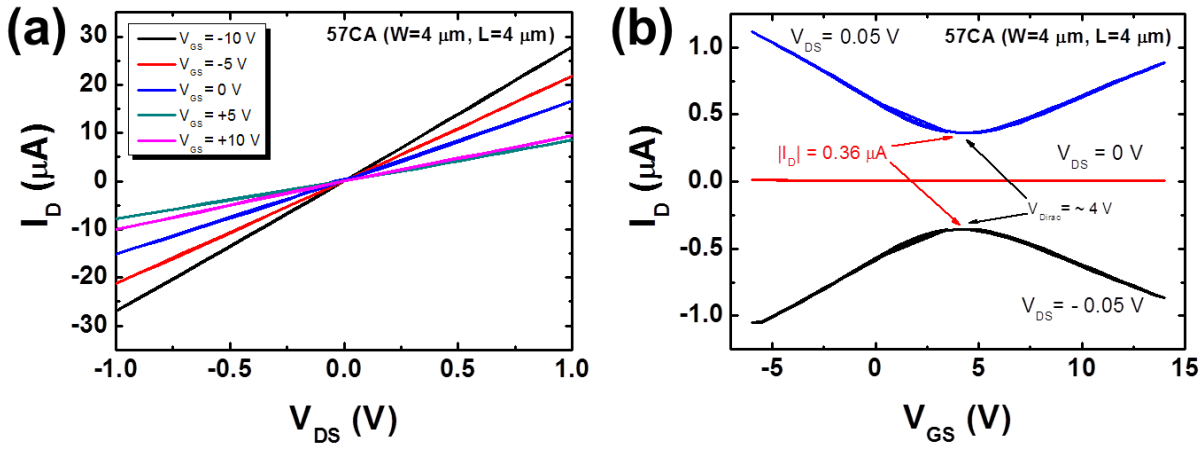


Figure 6.6 I_D-V_{DS} and I_D-V_{GS} characteristics of CVD growth graphene FETs.

variation for the V_{Dirac} and minimum current in spite of channel passivation by Al_2O_3 film. On the other hand, the length dependence of G-FETs is also observed with same channel width of 4 μm and the channel length is varying from 4, 5, 6, 7, 8, 10, and 12 μm. However, they show irregular behaviors as shown in Figure 6.7. It might be due the contact resistance becoming the major limiting factor for the graphene applications [254-256]. Therefore, an individual G-FET was selected for the detailed analysis.

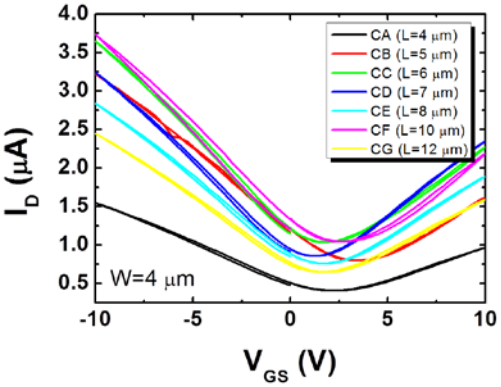


Figure 6.7 I_D-V_{GS} characteristics of G-FETs with different channel length.

6.3.2 Mobility scatterings on the SiO_2 substrate

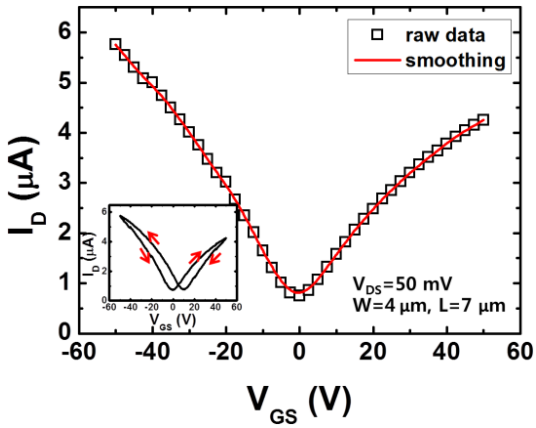


Figure 6.8 Single I_D-V_{GS} characteristic and hysteresis of a G-FET.

For the detailed analysis of a G-FET, one graphene device was chosen which have near-ideal V_{Dirac} with the drain voltage of 50 mV. The channel width and length is 4 and 7 μm. At first, the gate voltage was swept between -50 and 50 V to confirm the hysteresis. Figure 6.8 exhibits raw data and smoothed curve of an I_D-V_{GS} characteristic which has V_{Dirac} of 0 V and an inset represents the gate hysteresis of the G-FET. The

V_{Dirac} and the minimum current is extracted about -0.5 V and 8.13×10^{-7} A, respectively. The I_{on}/I_{off} ratio is estimated about 1 due to the existence of the minimum current and it is disturbing for the digital switching applications. Even though many studies report the physical model for understanding the graphene, there is no general electrical model for the graphene FETs. Herein, the electrical characterization of G-FET is performed based on the conventional electrical model for MOS structure which is defined as

$$I_D = \frac{W}{L}\cdot\mu_{eff}\cdot Q_G\cdot V_{DS}$$
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L}\cdot\mu_{eff}\cdot C_G\cdot V_{DS} \quad (6.5)$$

where μ_{eff} is the effective mobility, Q_G is the charge carriers in the graphene, and C_G is the total gate capacitance. In practice, the total gate capacitance C_G should be considered as the series combination of the oxide capacitance C_{OX} and the quantum capacitance C_Q of graphene, i.e., $C_G=C_QC_{OX}/(C_Q+C_{OX})$ [257]. The C_Q is related to the density of states of graphene near the Dirac point [258]. But, in this analysis with Equation 6.5, the C_G is assumed to be C_{OX}, i.e. $C_G\approx C_{OX}$ since the quantum capacitance measurement is not performed yet.

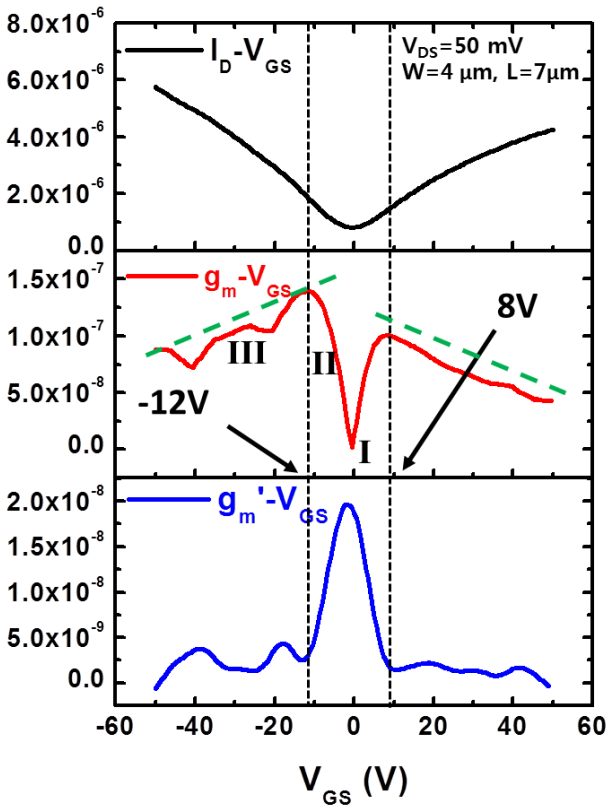


Figure 6.9 I_D, g_m, and $g_m'(=\partial g_m/\partial V_{GS})$ as a function of V_{GS} in the single layer G-FET.

The transport properties in the G-FET are confirmed between I_D-V_{GS} and g_m-V_{GS} curves as shown in Figure 6.9. The g_m' ($=\partial g_m/\partial V_{GS}$) is a reference to determine the slope of g_m at higher gate voltage. From the g_m-V_{GS} curve, the g_m first increases linearly (Region II) starting from the Dirac point (Region I) at lower gate voltage and then begins to decrease in reverse (Region III) at higher voltage (8 and -12 V for electron and hole, respectively). Interestingly, it is same for both of electron and hole carriers. The g_m at higher gate voltage is also linearly decreased as shown in g_m'-V_{GS} curve. In graphene, the carrier concentration can be determined from the integration of the density of states which increases

linearly with energy by the Fermi-Dirac distribution. In detail, based on Boltzmann theory, the conductivity σ_G for single-layer graphene is given by [259]

$$\sigma_G = qn\mu = q^2 v_F^2 D(E_F)\tau / 2 \tag{6.6}$$

where q is the electric charge, n is the carrier density, μ is the low-field mobility, v_F is the Fermi velocity ($\approx 10^6$ m/s), $D(E_F)$ is the density of states, and τ is the scattering time. The density of states $D(E_F)$ for single layer graphene is proportional to E_F

$$D(E_F) = \frac{2E_F}{\pi(\hbar v_F)^2} \tag{6.7}$$

where E_F is the Fermi energy is defined as $E_F \approx \hbar v_F \sqrt{\pi n}$ for single layer graphene. Hence, the charge carriers in single layer graphene Q_G should be increased as increasing the gate voltage. Despite of increase of carrier density at higher gate voltage, the reduction of current seems to be the mobility degradation limited by carrier scattering as already announced [225]. From this, it can be classified to three types of conduction variation region: Region I for the minimum current at the Dirac voltage, Region II for the linear increase in current region, and Region III for the mobility degradation region.

To observe the mobility behavior, the field-effect mobility defined as $\mu_{FE}=g_m L/(WC_{OX}V_{DS})$ was obtained the g_m and the effective mobility μ_{eff} is also calculated with the assumption for threshold voltage that is considered the V_{Dirac} as

$$\mu_{eff} = \frac{L}{WC_{OX}(V_{GS} - V_{Dirac})}\frac{I_D}{V_{DS}} \tag{6.8}$$

The comparison between the field-effect mobility and effective mobility is shown in Figure 6.10. The μ_{eff} is much larger value than the μ_{FE} and the maximum value of μ_{eff} is

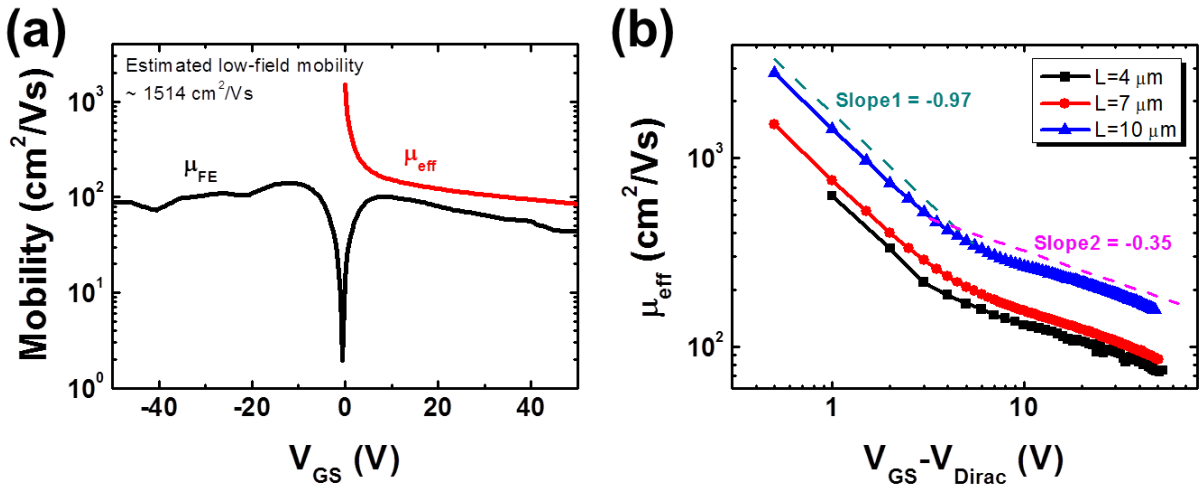


Figure 6.10 (a) Field-effect and effective mobility for G-FET. (b) Channel length dependence of μ_{eff}.

estimated about 1514 cm^2/Vs which is a similar value for other graphene devices on the substrate [260]. However, the mobility is dramatically degraded as increasing the gate voltage in proportional to $1/(V_{GS}\text{-}V_{Dirac})^{0.97}$ and $1/(V_{GS}\text{-}V_{Dirac})^{0.35}$. The behavior is appeared in same for different channel length as shown in Figure 6.10 (b). The mobility in single layer graphene is limited several scatterings which are mainly an acoustic phonon scattering and a substrate surface polar phonon scattering at room temperature. Using the Matthiessen rule, for the single layer graphene, the mobility can be expressed as [261]

$$\frac{1}{\mu_{Single}} \approx \frac{1}{\mu_C} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{OX}} \tag{6.8}$$

where μ_C is the Coulomb scattering, μ_{sr} the short-range scattering, μ_{AC} the acoustic phonon scattering, and μ_{OX} the substrate surface polar phonon scattering. Among them, the μ_C and μ_{sr} are the effective parameters at 4.2 K. The μ_{AC} and μ_{OX} are known to be in proportion to $1/nT$ and $1/n^{1/2}$, respectively where n is the carrier concentration [262]. For the surface polar phonon scattering, meanwhile it is less important in conventional MOSFETs but much more prominent in graphene due to the much smaller vertical dimension of the devices [259]. It is thought that the experimental results of mobility are similar to the theoretical dependence for the mobility scattering but it is not confirmed yet in here.

6.3.3 LF noise characteristics

Low-frequency noise in the G-FET was measured with different gate voltage. They show a general $1/f$ behavior for all different gate voltage and it is sensitive to the contact quality. If

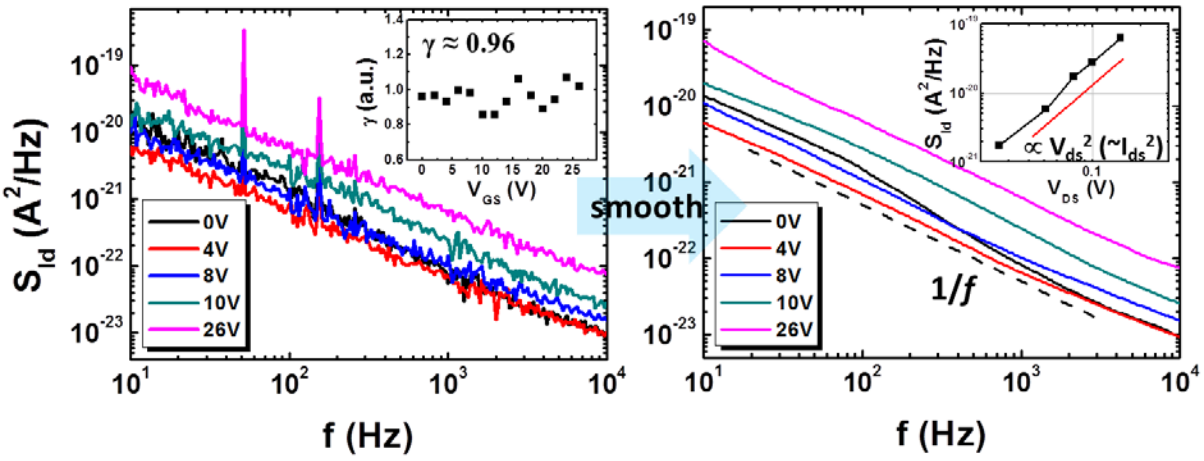


Figure 6.11 Drain current noise spectrum at V_{DS}=50 mV as a function of the frequency for the G-FET (W=4 μm, L=7 μm). The smoothed data appear the $1/f$ shape and the insets indicate the exponent of β and γ which are defined as $S_{Id} \sim I_D^{\beta}/f^{\gamma}$.

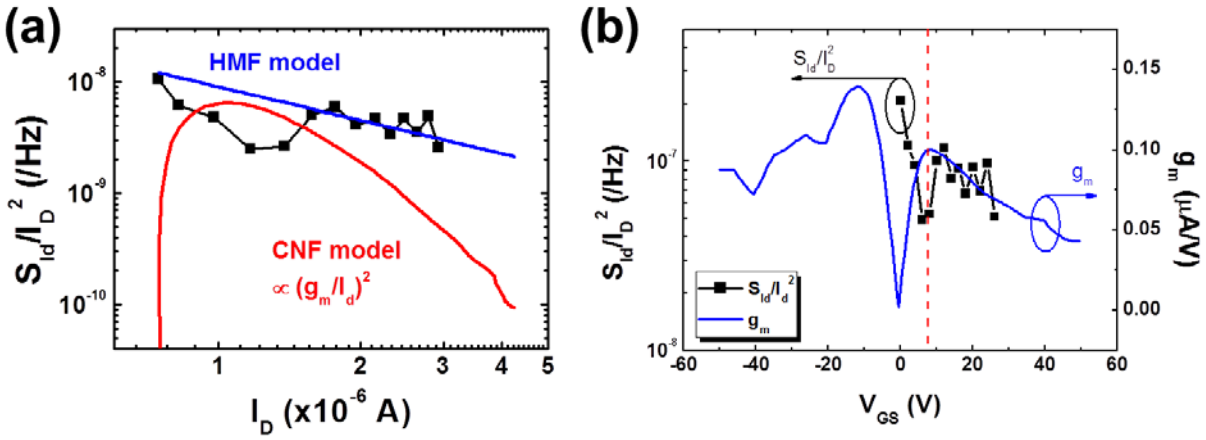


Figure 6.12 Comparison for the normalized drain current noise behavior in the G-FET (a) with the CNF and HMF model and (b) the transconductance g_m.

a probe does not make a good contact during the measurement, it exhibits a peculiar noise. In Figure 6.11, the raw and smoothed data of typical drain current noise power spectrum is shown. The insets show the extracted values of γ and β which are defined as I_D^{β}/f^{γ}. For the γ, it is about 0.96 and the noise S_{Id} is increased as proportional to I_{DS}^2 as changing the drain voltage since the drain current is linear to the drain voltage.

To confirm the noise origin, in the *n*-type region of G-FET, the normalized current noise was compared with the carrier number fluctuation (CNF) and the Hooge mobility fluctuation (HMF) model as shown in Figure 6.12 (a). The fitting curve of CNF model is made with the relation of $(g_m/I_D)^2$ from the I_D-V_{GS} characteristics but it is completely disagreed for the noise behavior in graphene. It exhibits that the noise is not originated from the carrier trapping and de-trapping at the graphene-oxide interface. On the other hand, the HMF model is also not fitted for whole region but it is partially fitted in the specific region that is away from the Dirac point. In Figure 6.12 (B), the noise behavior is compared to the behavior of g_m. Away from the Dirac point, the S_{Id}/I_D^2 is reduced as following $1/V_{GS}$ similar to the region III of g_m. However, near the Dirac point, it does not show a clear relation compared to the g_m.

As shown in Figure 6.13, the overall behaviors of the normalized noise involving both of *n*- and *p*-type region show the appearance of a M-shape that is similar to the previous reports [247], [248]. The M-shape behavior is a unique noise behavior only shown in single layer graphene. The drain current noise S_{Id} is incerased as increasing the gate voltage (i.e. carrier concentration) wheareas the normalized drain current noise S_{Id}/I_D^2 is decreased. Interestingly, the M-shape is similar to the behavior of g_m more clearly and the reduction of S_{Id}/I_D^2 show like the mobility degradation. In contrast, for multi layer graphene, it has been reported that

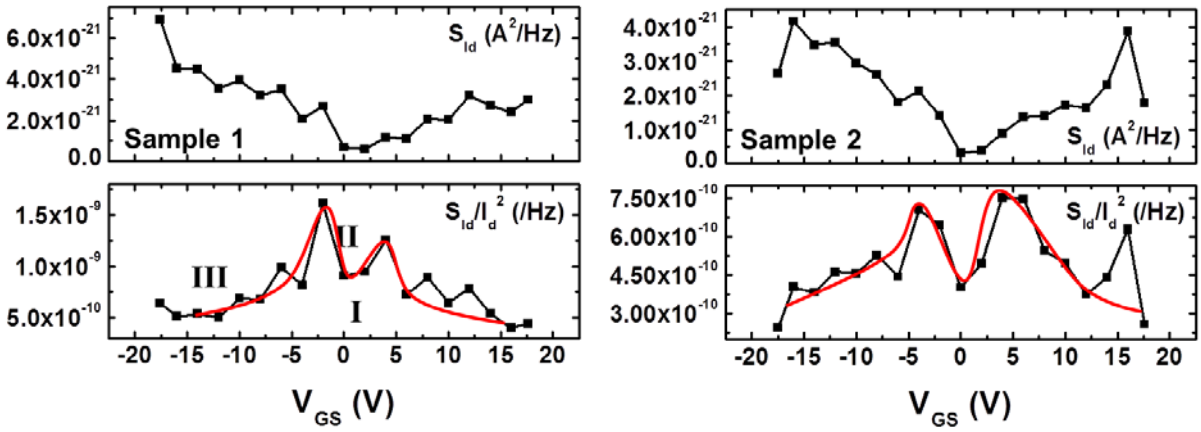


Figure 6.13 Drain current noise S_{Id} and the normalized drain current noise S_{Id}/I_D^2 for G-FETs. The behavior of S_{Id}/I_D^2 shows M-shape.

the normalized noise shows a V-shape as increasing the carrier concentration [247] and the mobility is also increased [261]. These difference trends for the mobility between single and multi layer graphene are due to the differences of density of states and the additional screening of the electric field of substrate surface polar phonons in multi layer graphene [261]. Away from the Dirac point, it seems that the 1/*f* noise in graphene is strongly correlated to the mobility scattering depending on the number of layer. It supports the partially fitted region by the HMF model. However, near the Dirac point, the noise origin is speculated to be same for single and multi layer graphene but it is not clear. The effect of spatial charge inhomogeneity near Dirac point is proposed [247].

6.4 Summary

Nowadays, graphene has been strongly interesting for various nanostructure applications due to its unique electronic structure and carrier transport. However, since the graphene has a zero band gap, there is no possibility for the conventional switching devices which have higher on/off ratio of the current by using graphene. Instead of that, the graphene is suggested as an ideal material for the radio frequency analog electronics, conducting transparent film, or photonic devices. Nevertheless, the field effect device structure with graphene is useful to understand the inherent transport properties of graphene and the impact on the environments such as the supporting substrate and the metal contact.

It has been well known that the carrier transport of graphene is strongly affected by elastic and inelastic scatterings. To understand these scattering mechanisms, various measurement

techniques are required such as the low-temperature, or Hall measurement. Low-frequency noise can be also a useful tool to help for understanding because the scattering is also one of important factors for the conductivity fluctuation. Therefore, in this section, the single layer graphene FETs based on the mechanical exfoliation and the CVD growth processes were studied using DC and LF noise measurement. Their electrical properties were analyzed with the electronic model for MOS structure. The G-FETs exhibit three kinds of different transport depending on the carrier concentration and the noise in low-frequency region appears in the shape of $1/f$. The noise was tried to be understood with the CNF and HMF model as changing the gate voltage so that it is partially fitted with the HMF model. It is not clear but LF noise in graphene might be deeply correlated to the mobility behavior and its scattering compared to the previous studied for the mobility in graphene.

Conclusion & Perspectives

Chapter 7 Conclusions & Perspectives

As the message that is given by R. Feynman, *'There is plenty of room at the bottom'*, low-dimensional structures opened up many possibilities for the micro and nano world with amazing physical properties ruled by the quantum mechanics. Recently, many studies for the low-dimensional structures have been performed to understand the transport properties and related effects for electronic applications by its electrical measurements such as *I-V* or *C-V* measurement. On the other hand, low-frequency noise generally observed in most of electronic devices is known to relate the carrier dynamics and the characterization has been used to give some information for the traps at the oxide. Even though the noise origin is not clear in all cases, there are well-known models to explain the noise based on conventional MOSFETs. In here, low-dimensional structures such as nanowires, nanotubes, and graphene were investigated in terms of transport properties and low-frequency noise characteristics for the FET structure. At first, the theoretical background for the study is summarized in previous three chapters and the experimental results is shown later.

As the beginning of theoretical background, in chapter 1, the current issues for device scaling in CMOS technology are written for understanding the low-dimensional structures about the meaning and necessity. Metal-oxide nanowires, carbon nanotubes, and graphene as well-known 1-D and 2-D structures are introduced and two representative approaches (top-down and bottom-up ones) for low-dimensional structures are compared. Their electrical issues in the viewpoint of transport and low-frequency noise are discussed for device applications.

In chapter 2, the important device parameters for FET structure such as threshold voltage, mobility, series resistance, subthreshold swing, and capacitance are discussed with the definition and practical extraction methods. For the threshold voltage, the pros and cons of several methods such as linear extrapolation, second derivative, and Y-function method are compared and the mobility is explained depending on the different physical ideas. In addition, other parameters to determine the device performance are introduced that are series resistance, subthreshold swing, and capacitance. All experimental parameters extraction and analysis was performed and understood based on these electrical characterization techniques.

The fundamentals and concepts of electronic noise are summarized for understanding low-frequency noise in FET structures in chapter 3. The electronic noise can be classified as thermal, shot, generation-recombination (g-r), random telegraph signal, and 1/*f* noise. Among them, the g-r and 1/*f* noise is well observed in electronic devices and the random telegraph signal noise especially for smaller device. They are called generally low-frequency noise because well observed in the low-frequency region. There are two representative noise models which are useful to explain the low-frequency noise for FET structure: one is the mobility fluctuation model suggested by Hooge and the other is the carrier number fluctuation model involving the correlated mobility fluctuations by trapped charge carriers at the interface. And then the practical system configuration and considerations for the noise measurement are introduced.

From chapter 4 to chapter 6, the experimental results for the transport properties and low-frequency noise are studied with multi-gate FETs, nanowire and nanotube devices, and graphene FET. The multi-gate FETs are noticeable device recently introduced to obtain the better gate control. A FinFET is well-known for the multi-gate structure having a surface conduction by channel inversion whereas a junctionless FET has a new device concept that is operated by the highly doped channel i.e. bulk conduction. The electrical properties and low-frequency noise between both devices are compared. Interestingly, the low-frequency noise in junctionless FET is explained by the carrier number fluctuation model same as the FinFET but the origin is rather different. For the FinFET, the fluctuations are owing to the carrier trapping and de-trapping at the oxide-semiconductor interface while the junctionless FET is not totally. So, in the junctionless FET, it might also come from the interface between the doped channel and depletion region, i.e. Schottky-Read-Hall generation-recombination.

In the case of nanowire and nanotube structures, the impact of strain and metal contact on the low-frequency noise is observed. First, 3-D stacked Si and SiGe nanowire gate-all-around FETs were compared between compressively strained and un-strained devices. Even if the c-strained SiGe shows the inhomogeneous trap distribution in long channel devices, the trap density of both devices is similar. However, the c-strained SiGe FETs effectively reduce the influence of correlated mobility fluctuations by trapped charge carriers compared to the un-strained ones. Moreover, the annealing process for Si nanowire FET makes it worse despite of the surface roughness reduction. And the influence of metal-semiconductor junction for noise is studied with different metal contacts based on the noise analysis. The existence of Schottky barrier shows different relationship between the low-frequency noise and the device

resistance. Hence, it indicates that contact metal for nanowire is important to understand the electrical properties. With low-frequency noise analysis, the quality of metal contact on the GaN nanowire is confirmed. It needs more studies to confirm it but it shows a potential to determine the device quality with low-frequency noise measurement.

Graphene is an interesting material that is perfect 2-D structure having surprising high carrier mobility, massless electrons, and a zero band gap. As focusing these transport properties, many researchers have studied for the applications. Even though the graphene was recorded a few hundred thousands of mobility, the graphene devices on the substrate exhibited much lower mobility due to the significant impact of scattering. Low-frequency noise in graphene is also discussed to understand the carrier dynamics. Indeed, since there is no electric model for graphene, the analysis is performed with conventional model. The LF noise in single layer graphene FETs exhibits M-shaped behavior of $1/f$ noise and it might be related to the transconductance variation limited by the mobility scattering. However, it still remains a suspect and needs more analysis with appropriate electronic model.

In this dissertation, it is shown that low-frequency noise measurement & characterization can be meaningful to understand carrier dynamics and assessment device reliability for low-dimensional structure applications. As decreasing the device size, the output current will decrease unquestionably but the noise is not diminished. Hence, in nano-scale devices, the noise study will be increasingly important for understanding and reducing. Moreover, some measurements (e.g. C-V measurement) are at the breaking point to understand nano-scale devices. Low-frequency noise in low-dimensional structures is impacted by the device architecture, the conduction mechanism, the channel strain engineering, and the metal-semiconductor junctions, and the 2-D channel structure. Most of noise studies are performed at room temperature but the studies of low-temperature noise measurement are not sufficient due to the effect of additional external noise by related equipment for the low-temperature system. Even though the noise origin is mainly due to the carrier trapping and release at the interface or in the dielectric, it is impossible to ignore the effect of carrier scattering on the noise. Hence, the noise measurement in low-temperature is also interesting to figure out the influence of carrier scattering on the noise for future work.

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Appendix I – Physical constants

Electronic charge	q	1.602×10^{-19} C
Speed of light in vacuum	c	2.998×10^{10} cm/s
Permittivity of vacuum	ε_0	8.854×10^{-14} F/cm
Free electron mass	m_0	9.11×10^{-31} kg
Plank's constant	h	6.625×10^{-34} J s
		4.135×10^{-15} eV s
Boltzmann's constant	k	1.38×10^{-23} J/K
		8.62×10^{-15} eV/K
Avogadro's number	A_0	6.022×10^{23} molecules
Thermal voltage	V_t	0.025860 V (300K)
		0.025256 V (293K)
Speed of light in vacuum	c	2.99792×10^{10} cm/s

Appendix II – Glossary & abbreviations

2DEG	two-dimensional electron gas
AC	alternating current
AFM	atomic force microscopy
c	velocity of light (2.998×10^{10} cm/s)
c_p	velocity of particle (cm/s)
c-strained	compressively strained
C	capacitance (F)
C_b	bulk capacitance (F/cm^2)
C_b	substrate depletion charge density (F/cm^2)
C_G	total gate capacitance (F/cm^2)
C_{GB}	gate-to-bulk capacitance (F/cm^2)
C_{GC}	gate-to-channel capacitance (F/cm^2)
C_i	inversion charge density (F/cm^2)
C_{it}	interface trap capacitance (F/cm^2)
C_{OX}	oxide capacitance (F/cm^2)
CESL	contact etch stop liners
CMF	correlated mobility fluctuation
CMOS	complementary metal-oxide-semiconductor
CNF	carrier number fluctuation
CNF+CMF	carrier number fluctuations with correlated mobility fluctuation
CNT	carbon nanotube
CVD	chemical vapor deposition
$D(E_F)$	density of states
DAQ	data acquisition
DC	direct current
DG-MOSFET	double-gate MOSFET
DIBL	drain induced barrier lowering
DLTS	deep-level transient spectroscopy
E_a	activation energy (eV)
E_{eff}	effective electric field (V/cm)
E_F	Fermi energy level (eV)
EOT	equivalent oxide thickness
f	frequency (Hz)
FD-SOI	fully depleted SOI
FE	field emission
g_d	drain conductance
g_m	transconductance
g-r	generation-recombination
G_Q	quantum capacitance (F/cm^2)
G-FET	graphene field-effect transistor
G4-FET	four-gate FET
GAA FET	gate-all-around FET

GNR	graphene nanoribbons
HMF	Hooge mobility fluctuation
$i(t)$	small-signal variables of current (A)
I	current (A)
I_0	average value of current (A)
I_D	drain current (A)
IC	integrated circuit
ITRS	international technology roadmap for semiconductors
KFM	kelvin probe force microscopy
L	channel length (cm)
L_{eff}	effective channel length (cm)
L_G	gate channel length (cm)
LF	low-frequency
m^*	effective mass of charge carrier (kg)
m_p	rest mass of particle (kg)
MOSFET	metal-oxide-semiconductor field-effect transistors
MWNT	multi-walled carbon nanotube
n	electron density (cm^{-3})
n_i	intrinsic carrier density (cm^{-3})
N	total number of free carriers
N_A	acceptor doping density (cm^{-3})
N_C	total number of charge carrier in the channel
N_d	donor doping concentration (cm^{-3})
N_{it}	interfacial oxide trap density ($cm^{-2}eV^{-1}$)
N_t	volumetric oxide trap density ($cm^{-3}eV^{-1}$)
NW	nanowire
p	hole density (cm^{-3})
p_m	mobile trapped charge
p_{ot}	oxide trapped charge
p_p	momentum of particle
PR	photo-resist
PSD	power spectral density (A^2/Hz or V^2/Hz)
q	electric charge (1.6×10^{-19} C)
Q_b	substrate depletion charge (C/cm^2)
Q_d	depletion charge (C/cm^2)
Q_f	fixed charge at the Si-SiO_2 interface (C/cm^2)
Q_G	charge carriers in the graphene (C/cm^2)
Q_i	inversion channel charge density (C/cm^2)
Q_{it}	interface trapped (or state) charge (C/cm^2)
QHE	quantum hall effects
R	resistance (ohms)
R_0	quantum resistance (ohms)
R_C	contact resistance (ohms)
R_{ch}	channel resistance (ohms)
R_D	drain resistance (ohms)

R_H	Hall coefficient (cm^3/C)
R_S	source resistance (ohms)
R_{SD}	series resistance (=R_S+R_D) (ohms)
R_{total}	total resistance (ohms)
RTS	random telegraph signal
S	subthreshold swing (V/decade)
$S(f)$	power spectral density
S_I	current noise power spectral density (A^2/Hz)
S_{Id}	drain current noise power spectrum (A^2/Hz)
S_R	resistance noise power spectral density (Ω^2/Hz)
S_V	voltage noise power spectral density (V^2/Hz)
S_{Vfb}	flat-band voltage spectral density (V^2/Hz)
S_{Vg}	input gate voltage spectral density (V^2/Hz)
S/D	source/drain
SEM	scanning electron microscope
SHG	second harmonic generation
SiO_2	silicon dioxide
SNR	signal to noise ratio
SOI	silicon on insulator
SRH	Shockley-Read-Hall
T	absolute temperature (K)
T_{Si}	thickness of silicon (cm)
TE	thermionic emission
TEM	transmission electron microscope
TFE	thermionic-field emission
TIL	thickness of interfacial layer
TLM	transmission-line method
V	voltage (V)
V_{bi}	built-in voltage (V)
V_{BS}	substrate-source voltage (V)
V_{Dirac}	Dirac voltage (V)
V_{DS}	drain-source voltage (V)
V_{FB}	flat-band voltage (V)
V_{GS}	gate voltage (V)
V_H	Hall voltage (V)
V_{SB}	source-substrate voltage (V)
V_{TH}	threshold voltage (V)
VLS	vapor-liquid-solid
W	channel width (cm)
W_{Fin}	fin width (cm)
W_{total}	total width (cm)
x_d	depletion width (cm)
α_C	Coulomb scattering coefficient (Vs/C)
α_H	Hooge constant
ε	relative permittivity

ε_0	vacuum permittivity
ε_{ch}	permittivity of channel material
θ_1	mobility attenuation factor related to series resistance
θ_2	mobility attenuation factor related to surface roughness
λ	tunneling distance (or attenuation length)
μ	carrier mobility
μ_0	low field mobility
μ_{AC}	mobility limited by acoustic phonon scattering
μ_{bulk}	bulk mobility
μ_C	mobility limited by Coulomb scattering
μ_{drift}	conductivity (or drift) mobility
μ_{eff}	effective mobility
μ_{FE}	field-effect mobility
μ_H	Hall mobility
μ_{OX}	mobility limited by substrate surface polar phonon scattering
μ_{SR}	mobility limited by surface roughness limited mobility
μ_{sr}	mobility limited by short-range scattering
ρ	resistivity
σ	conductivity
τ	average carrier scattering time (or carrier relaxation time)
τ_h	time constant in the higher state
τ_l	time constant in the lower state
ϕ_F	bulk potential
ϕ_S	surface potential
Φ_B	tunneling barrier height
Φ_M	work function of metal
Φ_S	work function of semiconductor

Appendix III – FlexPDE simulation script

FlexPDE source code for 20 nm FinFET structure simulation (http://www.pdesolutions.com)

```
TITLE                                   {FinFET.pde – 20 nm Fin width (IMEP-LAHC)}
        '20nm FinFET'                   {Doyoung, Ghibaudo}

COORDINATES
        cartesian

SELECT
        errlim= 1e-9
        STAGES=31
        nodelimit=100

VARIABLES
        V
        V1

DEFINITIONS
        q=1.6e-19
        k=8.6e-5
        T=300
        kT=k*T

        L=1e-4                          {channel length = 1um}
        wfin=20e-7                      {fin width ~ 10 to 1000nm}
        tsi=65e-7                       {sidewall thickness = fin height = 65nm}
        tox=1.7e-7                      {equivalent oxide thickness, Si = 1.7nm (HfSiO)}

        Nd=5e12                         {non-intentional doped Si channel}
        !Ng=1e10                        {gate doping}
        Nsd=2e20                        {source-drain doping}
        ni=1.4e10                       {intrinsic doping}
        lam=1.5e-7                      {quantum length}

        Vbi=kT*ln(Nd*Nsd/ni^2)
        !Vfb=-kT*ln(ni^2/Ng/Nd)

        eps0=8.85e-14                    {vacuum permittitivy}
        epssi=12*eps0                    {Si permittitivy}
        epsox=4*eps0                     {Oxide permittitivy}
        Cox=eps0*epsox/tox

        !mun=70+1090/(1+(Nd/1.26e17)^0.8)          musd=100
        mun=400                  musd=100

        eps=epssi

        n0=Nd
        p0=ni^2/Nd

        s=0
        s1=0

        E=-grad(V)
        Ex=-dx(V)
        Emag=abs(Ex)

        E1=-grad(V1)
        Ex1=-dx(V1)
        Emag1=abs(Ex1)

        !R=(1-exp(-((tox+wfin)^2+tsi^2-x^2-y^2)/lam^2))*ustep((tox+wfin)^2+tsi^2-x^2-y^2)
        R=1

        Ec=4e7
        Esr=3.27e13
        !mu=mun/(1+(Emag/Ec)+(Emag^2/Esr))

        Vg=1.5*(stage-1)/30
        Vd=0.01

        lambda=1e-8
        Nt=6e18
        Nit=Nt*lambda
        dQit=q*Nit

        mu=mun/(1+(Emag/Ec)+(Emag^2/Esr))
        mu1=mun/(1+(Emag/Ec)+(Emag^2/Esr))

        n=R*n0*exp(V/kT)
        p=R*p0*exp(-V/kT)

        n1=R*n0*exp(V1/kT)
        p1=R*p0*exp(-V1/kT)

        Qi=q*integral(n,2)
        Qi1=q*integral(n1,2)

        Id=Qi*mu*Vd/L
        Id1=Qi1*mu1*Vd/L
```

```
        RG=ln(Id1/Id)/dQit*Cox
        freq=20

        Sq=q*q*Nit*kT/freq
        SVfb=Sq/((wfin+tsi)*L*Cox^2)
        SIdN=RG^2*SVfb
        SIdHooge=1e-4/(freq*Qi/q*L)
        SIdsIdQ=(ln(Id1/Id)/dQit)^2*Sq/((wfin+tsi)*L)     ! simulated noise result


INITIAL VALUES
        V= 0
        V1=0

EQUATIONS
        V: div(eps*grad(V))=s
        V1: div(eps*grad(V1))=s1

BOUNDARIES

region 1                                                {Oxide}
        eps=epsox
        s=0         s1=0
        n=1         n1=1

        start   "Oxide" (-(wfin/2)-tox,0)               value(V)=Vg         value(V1)=Vg
        line to (-(wfin/2)-tox,tsi+tox)                 value(V)=Vg         value(V1)=Vg
        line to ((wfin/2)+tox,tsi+tox)                  value(V)=Vg         value(V1)=Vg
        line to ((wfin/2)+tox,0)                        natural(V)=0        natural(V1)=0
        line to close

region 2                                                {Silicon}
        eps=epssi
        s=q*(R*n0*exp(V/kT)-R*p0*exp(-V/kT)-Nd)
        n=R*n0*exp(V/kT)
        mu=mun/(1+(Emag/Ec)+(Emag^2/Esr))

        s1=q*(R*n0*exp(V1/kT)-R*p0*exp(-V1/kT)-Nd)
        n1=R*n0*exp(V1/kT)
        mu1=mun/(1+(Emag/Ec)+(Emag^2/Esr))

        start   "Si" (-wfin/2,0)                        natural(V)=0        natural(V1)=dQit
        line to (-wfin/2,tsi)                           natural(V)=0        natural(V1)=dQit
        line to (wfin/2,tsi)                            natural(V)=0        natural(V1)=dQit
        line to (wfin/2,0)                              natural(V)=0        natural(V1)=dQit
        line to close

region 3                                                {BOX}
        eps=epsox
        s=0         s1=0
        n=1         n1=1

        start   "Oxide" (-10e-7-(wfin/2),0)             natural(V)=0        natural(V1)=0
        line to (-10e-7-(wfin/2),-5e-7)                 natural(V)=0        natural(V1)=0
        line to (10e-7+(wfin/2),-5e-7)                  natural(V)=0        natural(V1)=0
        line to (10e-7+(wfin/2),0)                      natural(V)=0        natural(V1)=0
        line to close

PLOTS
        elevation(V) from (-(wfin/2)-tox,tsi/2) to ((wfin/2)+tox,tsi/2)
        surface (s/q) painted on region 2

        contour(V) painted on region 2
        contour(n) painted on region 2

        elevation(n-n0,p-p0) from (-(wfin/2)-tox,tsi/2) to ((wfin/2)+tox,tsi/2)
        elevation(mu,mun,0) from ((-(wfin/2)-tox)*0.99,tsi/2) to (((wfin/2)+tox)*0.99,tsi/2)

        elevation(log10(n),log10(p)) from (-(wfin/2)-tox,tsi/2) to ((wfin/2)+tox,tsi/2)

        elevation(s) from (-(wfin/2)-tox,tsi/2) to ((wfin/2)+tox,tsi/2)

SUMMARY
        report(Vbi)

HISTORIES

History(Qi) versus Vg
History(Id) versus Vg
History(log10(SIdN),log10(SIdsIdQ),log10(SIdHooge)) versus log10(Id)
History(mu,mun,0) versus Vg
History(Vg,mu) versus Vg            export format "#1   #2"         file="mu-Vg_20nm.txt"
History(Vg,Id,SIdN) versus Vg       export format "#1   #2   #3"   file="Vg-Id-SIdN_20nm.txt"


END   23969
```

Appendix IV – Wireless diagnosis system for nano-bio sensors

The wireless diagnosis system for nano-bio sensors is a research project that was performed from February to September for 8 months in 2008 with Min Kyu Joo, Yun Jeong Kim, and Gyu Tae Kim. A research purpose is the development of personal remote diagnosis system using nano-bio sensors which was fabricated with carbon nanotubes. The system will measure the current-voltage data of nano-bio sensors when a patient drop small amount of analytical reagent like saliva or blood of human body and transmit the data to mobile electronics such as PDA, laptop, and cellular phone for the analysis. It does not need to have all data to characterize the results because the data will be sent to mobile electronics and compare the accumulated data at the hospital or the disease center through an internet service. It can be able to make a portable size of remote diagnosis system which is convenient for the patients. In this research, the wireless diagnosis system has functions as following;

- Data transmission to PDA with wireless module (Bluetooth)
- Applying the voltage for drain and gate electrode
- Versatility for nano-bio sensors having large resistance range (50 kΩ ~ 20 MΩ)
- Multiple measurement for three nano-bio sensors
- Limitation of voltage source for the sensor protection

1. Hardware section of wireless diagnosis system

The diagnosis system consists of two parts of hardware, one is the main system for the data collection/transmission of nano-bio sensors and the other is electronics such as PDA which can be receive the data and connect to the internet service. Figure A-IV.1 shows a prototype of wireless diagnosis system and a PDA having software for the data collection. HP IPAQ 112 Classic Handheld as the PDA part was chosen among commercial products having a Bluetooth module and supporting the serial communication. But the diagnosis system can be extended to the other commercial products such as mobile phone, laptop supporting Bluetooth as well as PDA.

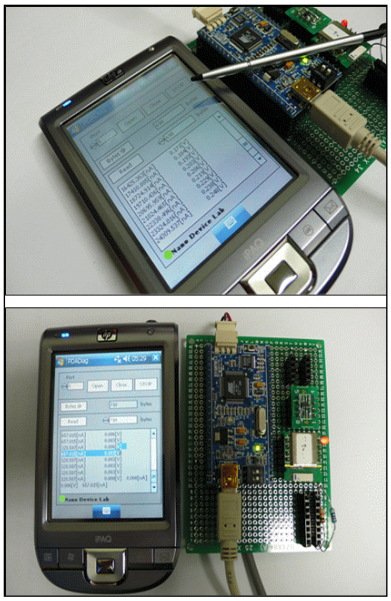

Figure A-IV.1 Image of prototype of wireless diagnosis system.

For the wireless communication of main system for nano-bio sensors, a commercial Bluetooth module (Parani ESD-200) supporting the serial communication was also used. The transmission distance is about 30 m without any extra antenna and empowered with 3.3 V voltage source. The programmable voltage source for the drain and gate electrode of nano-bio sensors was configured with two Digital to Analog Converter (DAC). At first, the DAC model number 'DAC7512' that can be apply positive voltage up to 3.3 V was chosen but it was altered to 'MAX5312' for higher positive/negative voltage supply (up to ±10 V). The output voltage of DAC is controlled by self-developed software so that the measurement condition can be tuned with a high accuracy in any situation. Bluetooth module and DAC are controlled by ARM7 microcontroller and ADC in ARM7 is also used for the current measurement. In here, lower power consumption logic was not considered.

Figure A-IV.2 exhibits the flowchart of wireless diagnosis system. Each module for applying voltage, reading current, and data transmission was organized in the first version of wireless diagnosis system. To optimize the system, we designed a printed circuit board (PCB)

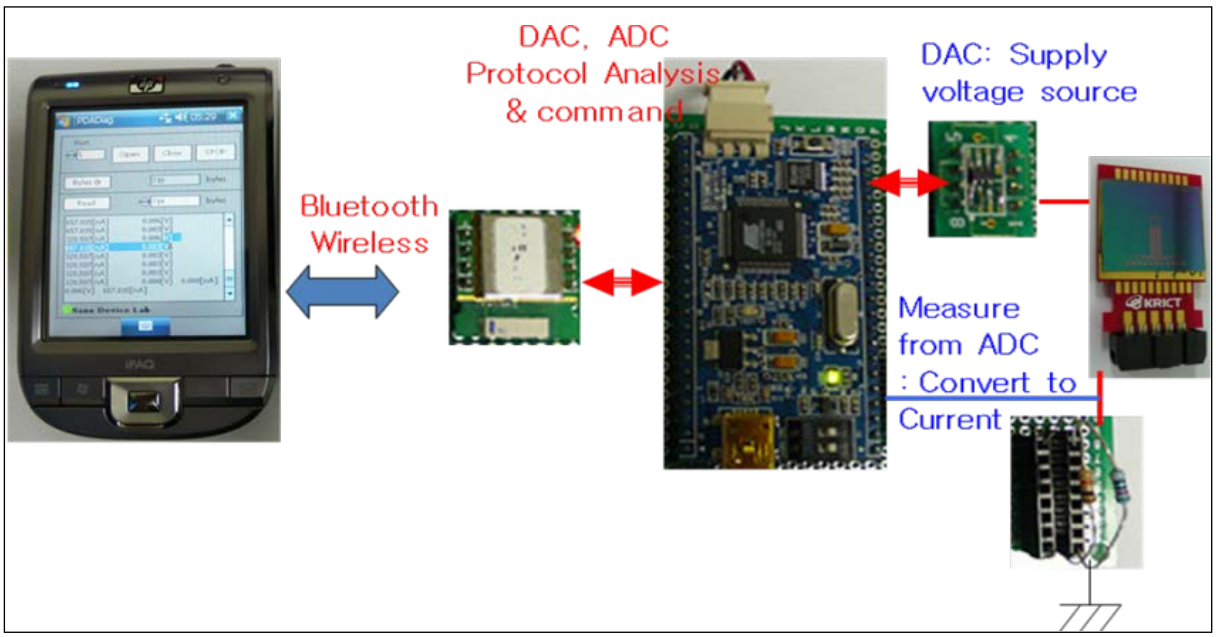

Figure A-IV.2 Schematic of overall process for the wireless diagnosis system. The system consists of wireless module, voltage supply (DAC), current reading (ADC), and mobile electronics

which is smaller and more stable by OrCAD (Cadence). Figure A-IV.3 shows a circuit design for PCB version of system.

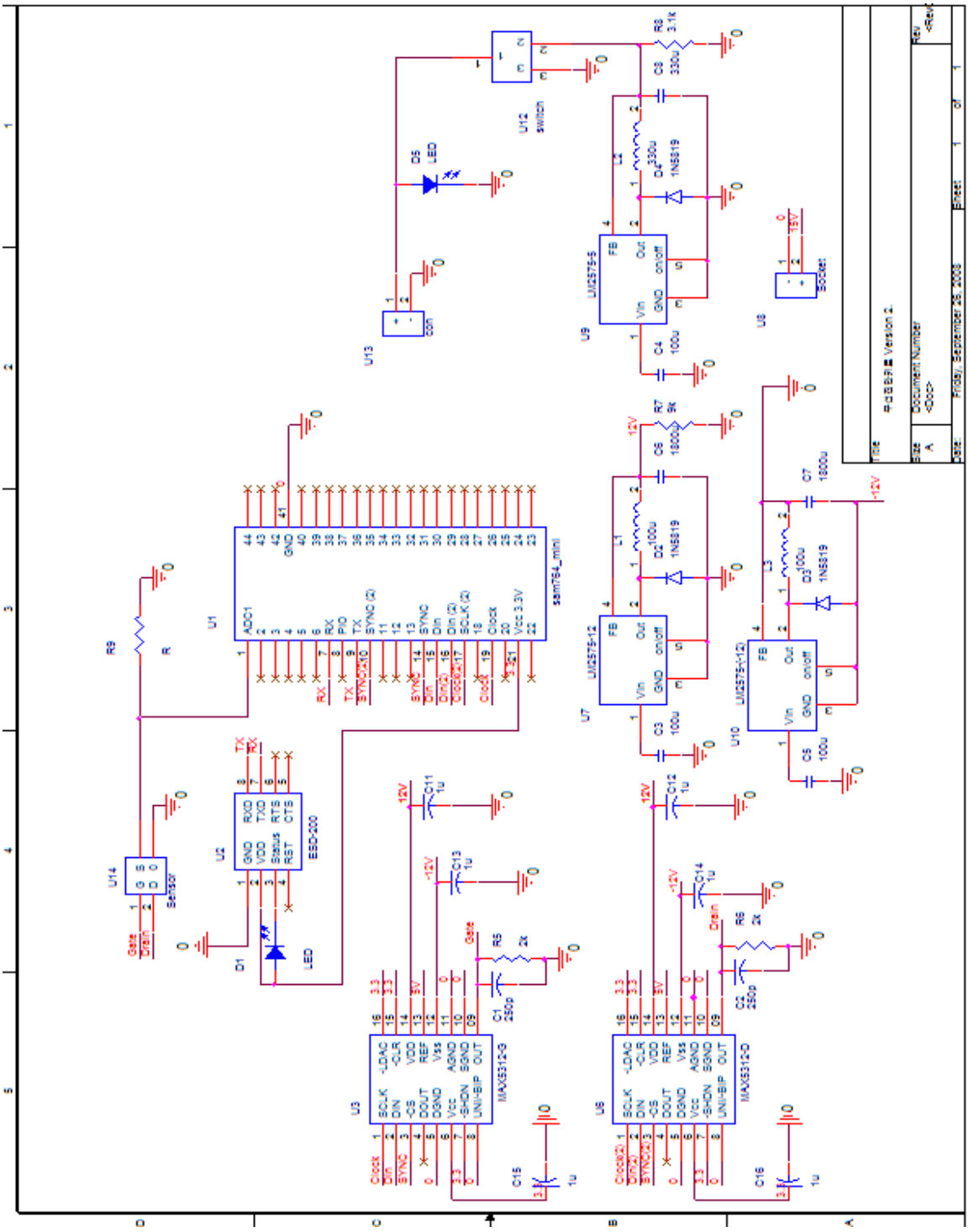

Figure A-IV.3 Schematic of circuit design for PCB version

2. Development of software for wireless diagnosis system

To communicate the manufactured hardware with PDA, controlling software is needed in the PDA system. For the wireless diagnosis system, two kinds of software were developed. One is for driving the system and the other is only for PDA (Windows Mobile). Figure A-IV.4 indicates the software framework for the wireless diagnosis system. The control software for the system was developed using C language because the microcontroller is optimized for the C language. The system software was loaded on the flash memory of controller. This kind of software cannot be modified easily by user because this program is low level frame and essential. But it is possible that the software upgrade and the extension of the function.

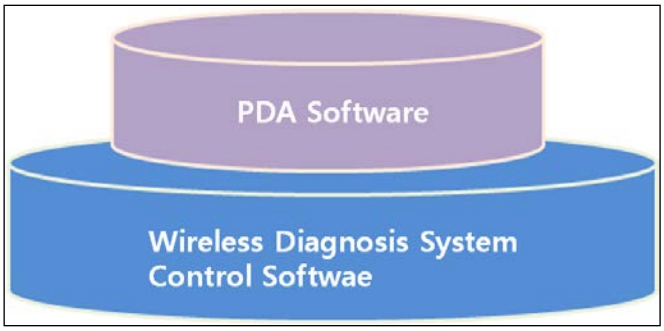

Figure A-IV.4 Software framework for wireless diagnosis system

Contrary to the system software, the purpose of the PDA software is the communication with the wireless diagnosis system. Therefore, it should have the graphical user interface (GUI) for sending commands and receiving data from the system. For this, LabVIEW 7.1 and Pocket PC PDA module are used to develop the PDA software. Figure A-IV.5 shows received data from the developed PDA software (left) and the other commercial serial communication software (right).

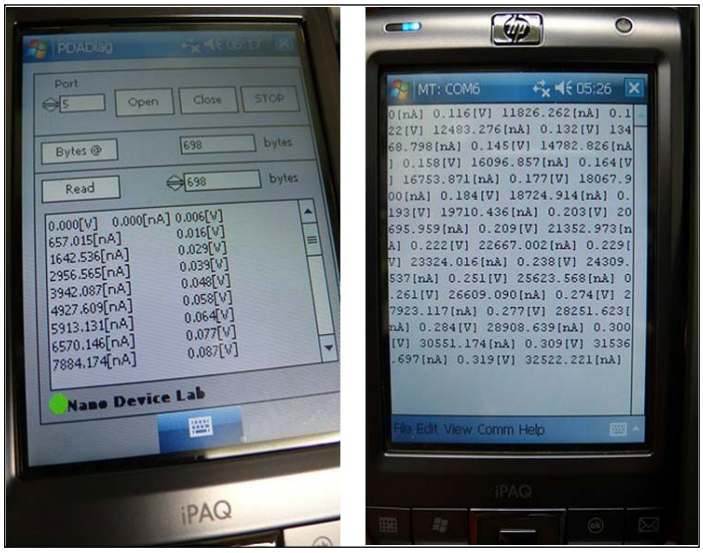

Figure A-IV.4 Software framework for wireless diagnosis system

In conclusion, the wireless diagnosis system was successfully demonstrated for nano-bio sensors. It cannot be used only for medical purpose but also for the research test in various environments using the wireless communication. It is applicable for the gas sensor without an additional cost.

Résumé du travail de thèse en Français

I. Introduction

La réduction d'échelle ('down-scaling' en anglais) est depuis toujours la force motrice de la technologie CMOS (complementary metal-oxide-semiconductor), en particulier en ce qui concerne la réduction de la consommation électrique, la largeur d'intégration des dispositifs, les coûts, l'accroissement de performance. Depuis peu ces réductions d'échelles on donné lieu à la réalisation de structures unidimensionnelles. On peut notamment mettre en avant différents points gouvernant cette réduction d'échelle : les dimensions, la vitesse, le rapport signal sur bruit. En particulier le signal de sortie des dispositifs électroniques doit être suffisamment important pour pouvoir le distinguer du bruit de fond. On peut ainsi noter un intérêt croissant dans l'étude du bruit électronique dans les structures de basse dimensionnalité. Dans le cas des transistors conventionnels MOSFETs (metal-oxide-semiconductor field-effect transistors), il est bien connu que le bruit basse fréquence est lié au piégeage et dépiégeage des porteurs à l'interface oxyde-semi-conducteur. Toutefois, pour les structures de faible dimensionnalité, les propriétés de ces dispositifs en termes de bruit n'ont pas été suffisamment étudié.

Dans cette thèse, nous nous intéressons aux propriétés de transport et au bruit basse fréquence dans des structures à effet de champ ('FET') de faible dimensionnalité fabriquées par des approches classique, descendantes ('top-dow'), ou des approches plus innovantes dites ascendantes ('bottom-up'). Nous focalisons notamment cette étude sur les diélectriques de forte constante diélectrique ('high-k'), les mécanismes de conduction, l'ingénierie de contrainte, les problématiques de contact métallique, les effets de diffusion des porteurs, comme schématisé sur la Figure 1. En premier lieu nous étudions deux types de transistors multi-grilles : le premier, le FinFET, est bien connu pour avoir une conduction de surface à travers l'inversion de canal, tandis que le second, de conception très récente, le transistor sans jonction ('junctionless FET') fonctionne sur le principe d'un canal fortement dopé, et donc par une conduction de volume. Pour la conduction de volume, nous pourrions nous attendre à un bruit provenant de fluctuations de la mobilité des porteurs. Or dans les structures sans jonction, nous pouvons analyser le bruit basse fréquence à partir d'un modèle basé sur la

fluctuation du nombre de porteurs de façon similaire à celui des transistors FinFET. Nous proposons différents mécanismes pour définir l'origine de ces sources de bruit. En ce qui concerne le FinFET, le bruit provient bien du piégeage et dépiégeage à l'interface oxyde-semiconducteur, alors que le bruit dans le transistor sans jonction est issu du piégeage des porteurs à la frontière entre le canal de conduction et la région de désertion. En ce qui concerne les strucutres de type nanofils et les nanotubes, nous avons pu observer l'impact de la contrainte mécanique sur le canal de conduction, ainsi que l'influence du contact métallique sur le bruit basse fréquence. Nous avons aussi comparé des structures tridimensionnelle transistors à effet de champ avec grille enrobante constitués de nanofils de type cœur-coquille empilés, avec ou sans contrainte compressives. Bien que les dispositifs contraints aient une distribution inhomogène des pièges le long du canal, les densités de pièges dans les deux types de dispositifs sont très similaires. Toutefois dans le cas des structures contraintes on note une réduction significative de l'influence des fluctuations de mobilité corrélées du fait du confinement des porteurs loin de l'interface oxyde/silicium. Ensuite, nous avons étudié l'influence de la jonction métal-semiconducteur avec plusieurs contacts métalliques à partir d'une analyse du bruit basse fréquence. L’existence d'un barrière Schottky provenant de la différence des travaux de sortie des matériaux induit des caractéristiques différentes pour le bruit basse fréquence et la résistance du dispositif. Ceci indique que le contact métallique avec un nanofil peut fortement affecter les propriétés de bruit dans des strucutres de faible dimensionnalité. En utilisant des mesures de bruit basse fréquence, nous pouvons analyser la qualité du contact métallique dans des nanofils de GaN, montrant que les techniques de mesure de bruit peuvent se révéler être un outil d'un grande utilité pour déterminer la qualité et la fiabilité des dispositifs. Par ailleurs en tant que structure 2D idéale, le Graphène est un matériau intéressant qui a des mobilités de porteurs extrêmement élevées, des masses d'électron nulles et sans bande interdite. Toutefois les transistors en Graphène qui sont réalisés sur substrat ont une mobilité de porteurs très fortement dégradée du fait de la diffusion importante des porteurs. Nous avons étudié le bruit basse fréquence dans ce genre de dispositifs en prenant en considération l'influence du substrat sur le canal de Graphène. Dans des transistors à monocouche de Graphène, le bruit a une caractéristique en forme de 'M' en fonction de la tension appliquée, et son comportement est semblable à la variation de transconductance limitée par la diffusion du substrat.

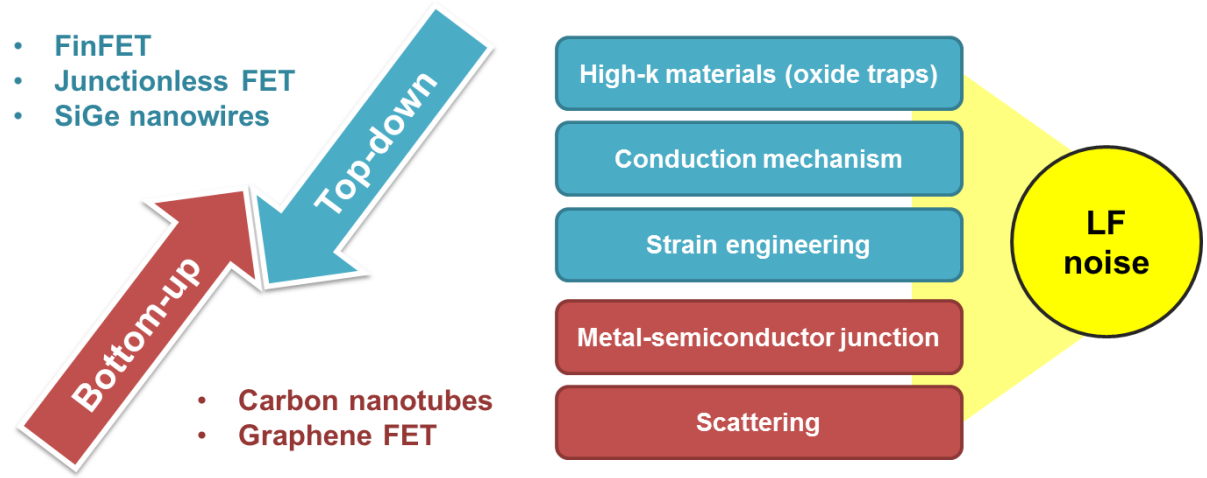

Figure 7 Schéma des objectifs de recherche: la compréhension de bruit à basse fréquence dans les nanostructures.

II. Propriétés de transport et bruit basse fréquence dans les transistors à effet de champ multigrilles : comparaison des mécanismes de conduction dans les FinFET et les transistors sans jonction

Nous avons comparé les résultats expérimentaux des transistors FinFETs et des transistors sans jonction en fonction de la largeur du canal. Les deux dispositifs ont été fabriqués en utilisant un substrat de type silicium sur isolant. Dans le cas du FinFET, un canal de silicium non-intentionnellement dopé a été réalisé en réduisant l'épaisseur (T_{Si}) à 65 nm. Les régions source/drain (S/D) étant dopées n^+ à quelques 2×10^{20} cm^{-3}. Un oxyde de grille de type HfSiO fa été déposé, avec une épaisseur d'oxyde équivalent de l'ordre de 1,7 nm. Une couche de 5 nm de TiN, encapsulée par une couche de 100 nm de poly-Si, a été utilisé comme électrode de grille. Par contre pour le transistor sans jonction, le canal a été dopé uniformément n^+ incluant les régions source/drain, de sorte qu'il n'y ait aucune jonction entre le canal et la région S/D. Dans ces structures, une couche de 10 nm de SiO_2 a été obtenue par croissance thermique, et une couche dopée p^+ de poly-Si a été utilisée comme électrode de grille. La Figure 2 montre une coupe longitudinale montrant le profil de dopage, les régions de conduction et des images par microscopie électronique à transmission (TEM) des deux types de dispositifs.

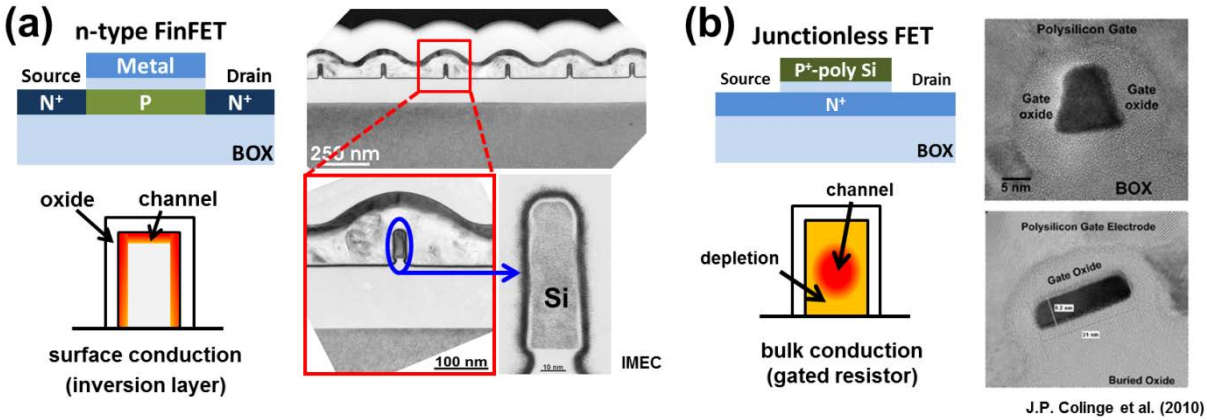

Figure 8 Longitudinal section transversale des profils de dopage, le profil de concentration d'électrons, et au microscope électronique à transmission (TEM) des images de (a) d'inversion de mode FinFET high-k/metal-gate (limitée par conduction de surface) et (b) plusieurs junctionless TEC à grille ayant de conduction de volume.

Pour un transistor de type FinFET, avec une largeur W_{Fin}=10 nm, nous avons obtenu, pour plusieurs tensions de grille V_{GS}, le spectre de puissance en fonction de la fréquence de la

Figure 3 (a). Ils combinent de comportements de type Lorentzien et 1/f. Pour des tensions V_{GS} < ~1.2 V, S_{Id} a un comportement proche d'une Lorentzienne qui est typique d'un bruit de type génération-recombinaison (g-r) ou signal télégraphique RTS (random telegraph signal), mais qui change pour un comportement de type bruit 1/f pour des tensions V_{GS} plus importantes. Afin de mieux comprendre l'origine du bruit basse fréquence dans les transistors de type FinFET, la densité spectrale de puissance S_{Id} a été normalisée par I_D^2. Si l'origine du bruit provient des fluctuations de porteurs, S_{Id}/I_D^2 devrait être proportionnel à $(g_m/I_D)^2$, alors qu'ils doit décroître selon l'inverse du courant de drain s'il s'agit de fluctuations de mobilités selon le modèle de Hooge (HMF). Par ailleurs, nous avons pris en compte les largeurs totales de canaux de conduction dans notre analyse en multipliant S_{Id}/I_D^2 et en divisant I_D , puisque le bruit et le courant dépendent de la largeur du canal. La Figure 3 (b) montre que les densités spectrales de bruit normalisée pour différents transistors FinFET de type n et de type p ont des comportements similaires. Pour les deux dispositifs nous pouvons noter l'apparition d'un plateau en dessous du seuil de conduction, qui décroit fortement lorsque le courant augmente. Ces résultats démontrent clairement que l'origine du bruit basse fréquence dans les FinFETs provient de fluctuations du nombre de porteurs à l'interface oxyde-semiconducteur, quel que soit le type de dispositif.

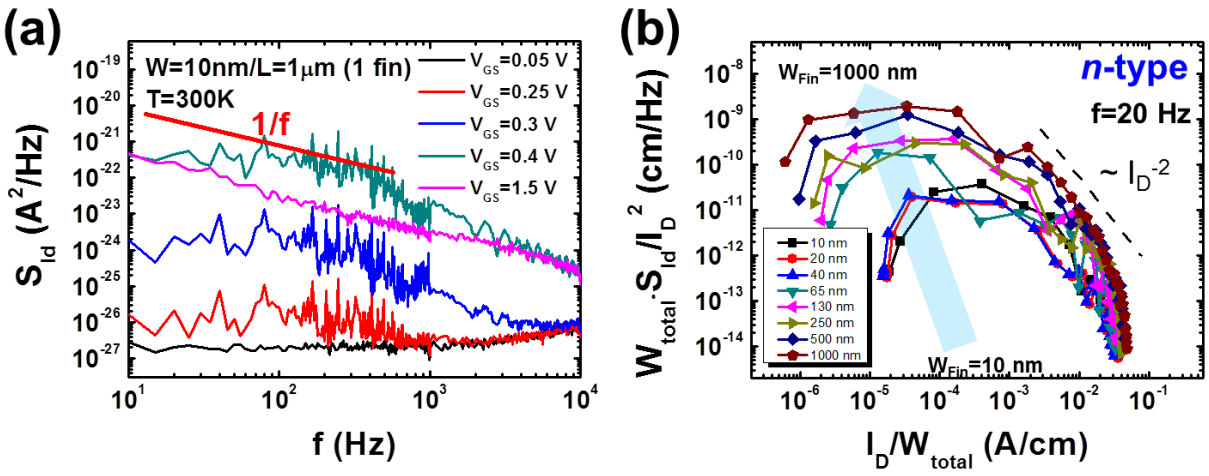

Figure 9 (a) des spectres de puissance de bruit actuel en fonction de la fréquence pour l'FinFET fonction de la tension de grille. (b) les densités spectrales de bruit normalisée pour différents transistors l'FinFET de type n et de type p ont des comportements similaires.

Comme nous pouvons l'observer sur la Figure 4, nous avons pu extraire la densité de pièges (N_t) ainsi que le coefficient de diffusion de Coulomb (α_C) en fonction de la largeur des dispositifs FinFETs. Pour les grandes largeurs de canal, ces densités sont de l'ordre de 2×10^{20}

$cm^{-3}eV^{-1}$ et décroissent avec la réduction de W_{Fin} pour finalement saturer à quelques 1×10^{19} $cm^{-3}eV^{-1}$ pour les canaux les plus étroits. Nous avons également observé une variation de N_t comme illustré sur la Figure 4 (a). Il semblerait que les densités de pièges N_t dans les dispositifs de type p soient légèrement plus importantes que pour les dispositifs de type n, mais les distances tunnel pour les électrons et pour les trous sont différentes. De ce fait, les densités de pièges pourraient être similaire si l'on considère que la distance tunnel pour les électrons est plus grande que pour les trous. Toutefois cela n'a pas d'impact significatif sur le coefficient de Coulomb α_C qui est de l'ordre de 10^3 Vs/C, qui décroit avec la largeur du canal W_{Fin}. Ceci pourrait être causé par les charges piégées sur les côtés du FinFET.

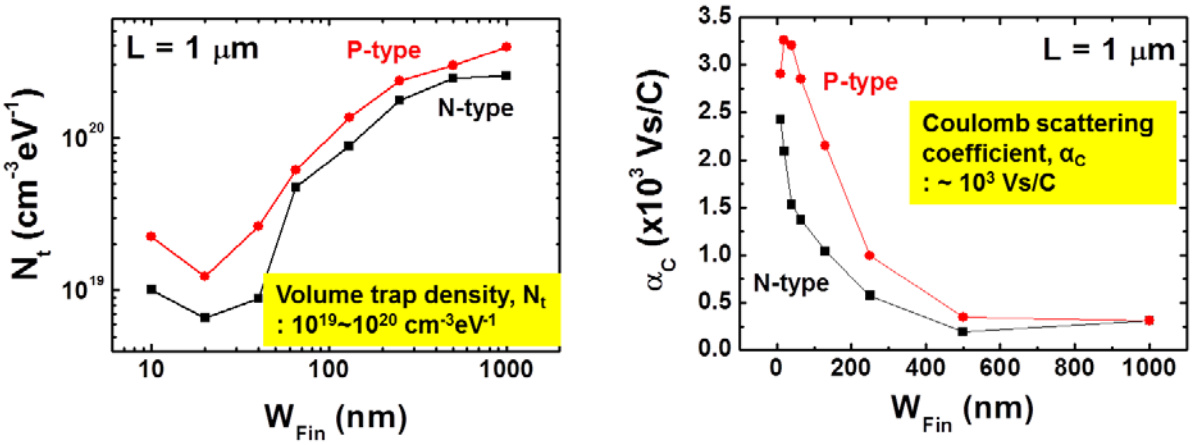

Figure 10 (a) la densité de pièges de volume et (b) coefficient de diffusion de Coulomb en fonction de la largeur de la nageoire FinFET sur la base du CNF + CMF.

Le transistor FET sans jonction est, de manière simplifiée, équivalent à un transistor en mode d'accumulation avec un canal de dopage identique aux source et drain. Sous le seuil, le transistor FET sans jonction est régime de désertion totale. Si la section du canal est suffisamment étroite, la grille peut alors entièrement dépléter le canal (i.e. dans l'état 'off') du fait de la différence des travaux de sortie entre le canal et l'électrode de grille. Au-dessus de la tension de seuil, le courant circule dans le volume du silicium qui est au centre du canal, et un canal d'accumulation peut alors se former si la tension de grille est suffisamment augmentée. Ainsi ce type de transistor possède des avantages conséquents par rapport aux dispositifs de conduction de surface, puisqu'il est a priori moins affecté par la dégradation de mobilité et des pentes de sous-seuil moins dégradées. La conduction est principalement limitée à la zone volumique à l'inverse des MOSFETs conventionnels à mode d'inversion du canal. En ce qui concerne la modélisation du bruit, on peut donc s'attendre à ce que la conduction de volume

dans ce type de transistors sans jonction affecte différemment le bruit basse-fréquence par rapport aux dispositifs à conduction de surface. Toutefois les transistors sans jonction ont aussi un conduction de surface additionnelle lorsque la tension de grille dépasse la tension de bandes plates. De plus il est bien connu que dans les dispositifs nanométriques le ratio surface/volume est plus important que dans les dispositifs classiques, mettant alors en avant l'importance des effets de surface dans ce genre de structures. Nous avons étudié le bruit 1/f dans les transistors sans jonction en traçant en échelle log-log la densité de puissance normalisée S_{Id}/I_D^2 en fonction du courant I_D , comme représenté sur la Figure 5. Le spectre de bruit prédit par le modèle CNF+CMF est validé sur une large gamme de tensions, à la fois sous et après le seuil. Le bruit prédit par le modèle de Hooge (HMF) n'est visiblement pas en mesure de prédire correctement la dépendance du bruit basse-fréquence du courant de drain.

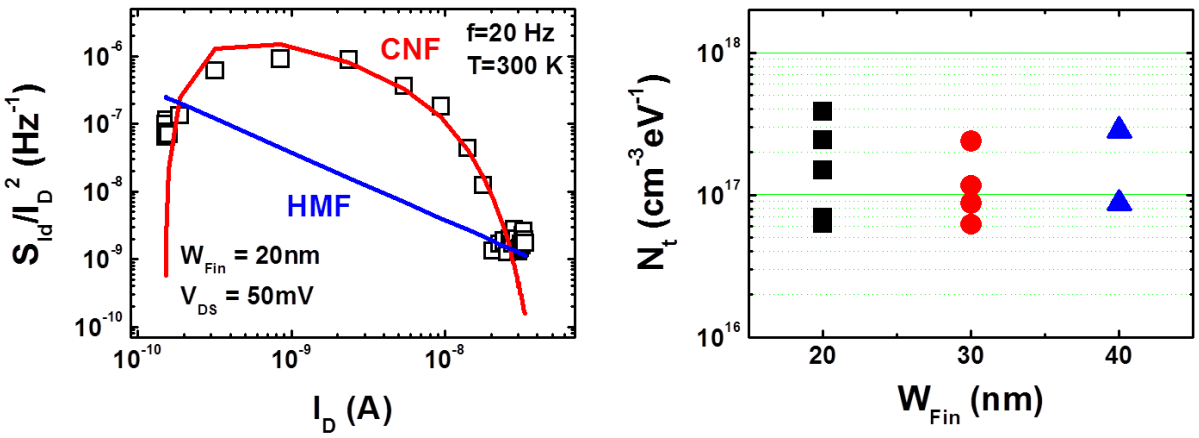

Figure 11 (a) Comparaison des CNF + CMF et HMF modèle pour W_{Fin} = 20 nm et (b) la densité extrait piège volume de le transistor FET sans jonction avec W_{Fin} différente.

En nous basant sur le modèle CNF+CMF nous avons pu calculer la densité de pièges N_t ainsi que le coefficient de Coulomb α_C. Ceci permet ainsi d'apporter des éléments d'information intéressants sur la qualité de l'interface d'oxyde, mais aussi sur les fluctuations de mobilité corrélées. Nous pouvons estimer N_t à quelques 6×10^{16} à 3×10^{17} $cm^{-3}eV^{-1}$ en considérant une longueur tunnel dans l'oxyde de $\lambda = 1\times10^{-8}$ cm. On retrouve ainsi des valeurs très semblables à celles des transistors classiques, mais considérablement meilleures que celles des transistors à forte constante diélectrique (high-k MOSFETs) qui sont typiquement de l'ordre de $N_t=10^{19} \sim 10^{20}$ $cm^{-3}eV^{-1}$. La valeur de α_C se situe autour de 1.1×10^4 à 5.1×10^5 Vs/C, indiquant que les fluctuations de mobilités corrélées jouent un roloe important dans les régions de fort courant. Nous pouvons supposer que ces fluctuations de mobilité sont dues à

des diffusions coulombiennes par les pièges chargés.

Malgré une bonne description des caractéristiques de bruit des transistors sans jonction par le modèle CNF+CMF, il est difficile de comprendre l'effet des pièges à l'interface oxyde-semiconducteur dans la région sous le seuil, car les interfaces silicium-oxyde de grille sont désertées dans ce régime, et les chemins de conduction se situent au centre du nanofil, loin des interfaces avec l'oxyde de grille. Une explication plausible est qu'il y a des fluctuations de l'épaisseur du canal dans le régime sous le seuil, lorsque le dispositif est partiellement déserté. Cet effet pourrait provenir de la présence de centres de génération/recombinaison Shockley–Read–Hall (SRH) dans la région de transition de Debye, entre le canal neutre et la région de désertion. Cet effet a aussi été observé dans les transistors à jonction et dans les transistor à quatre grilles (G^4-FETs).

Comme illustré sur la Figure 6 pour un FinFET, la densité spectral de puissance S_{Id} décroit graduellement lorsque l'on accroît la tension de grille V_{GS}. Ceci représente une relation entre S_{Id} et le courant de saturation dû à des effets de surface. Par ailleurs pour le transistor sans jonction, on observe un pic de bruit près le la tension seuil, relié au bruit G-R dû aux génération-recombinaison Schottky-Read-Hall. Ensuite, le bruit du courant de drain s'accroît à nouveau avec l'augmentation de la tension de grille V_{GS} , avec la formation d'un canal d'accumulation à la surface.

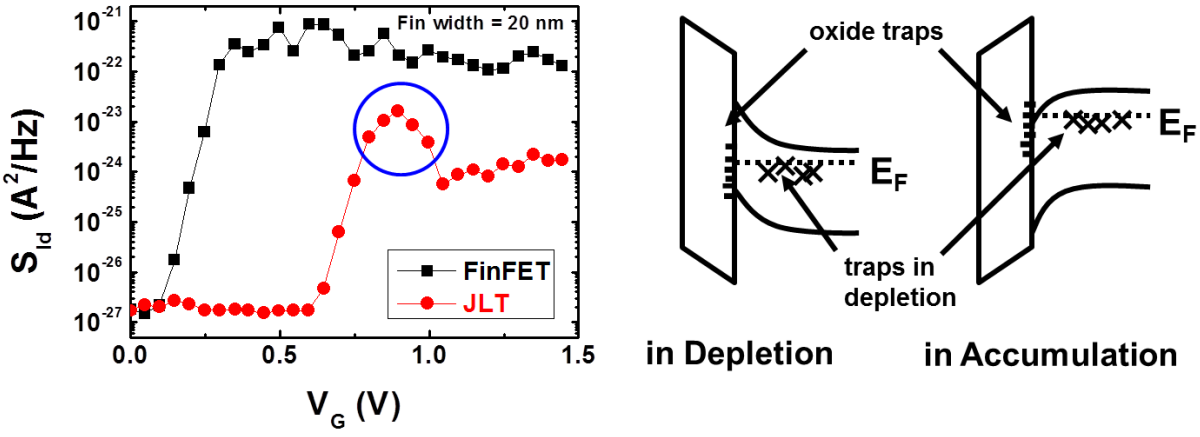

Figure 12 La densité spectral de puissance S_{Id} décroit graduellement lorsque l'on accroît la tension de grille V_{GS} .

En conclusion, nous avons étudié le rôle des mécanismes de conduction sur le bruit basse-fréquence par des analyses électriques et de bruit dans des transistors FETs multigrilles. Le bruit basse-fréquence dans les deux types de dispositifs étudiés est bien expliqué par le

modèle de fluctuation de porteurs (CNF) bien leur origine soit différente. Dans le cas du FinFET, le bruit basse-fréquence a pour origine le piégeage et dépiégeage des porteurs à l'interface oxyde-semiconducteur comme dans le cas des transistors conventionnels en mode d'inversion. Toutefois pour les transistors sans jonction le bruit basse-fréquence pourrait provenir de la charge de génération-recombinaison à la frontière entre la région du canal et celle de la zone de désertion.

III. Impact de la contrainte mécanique et du contact métallique sur le bruit pour des dispositifs à nanofil ou nanotube

A. Transistors à nanofils SiGe de type p empilés en 3D

En se basant sur l'approche 'top-down', les transistors à nanofils (NW) de type grille enrobante (Gate-all-around ou GAA) sont des candidats prometteurs pour les technologies MOS avancées. Ils offrent en effet de nombreux avantages, comme l'amélioration des performances électrostatiques qui dominent les effets canaux courts, avec une meilleure intégration en termes de densité du fait de leur structure d'empilement tridimensionnelle (3D). Nous présentons les propriétés électriques et les caractérisation de bruit basse-fréquence de transistors à nanofils 3D avec une grille à isolant de forte permittivité. Ces transistors Si (NMOS) et SiGe (PMOS) ont été réalisés par le CEA-LETI (France), par une méthode basée sur une combinaison de gravures anisotropiques et isotropiques lors de la mise en forme de la grille.

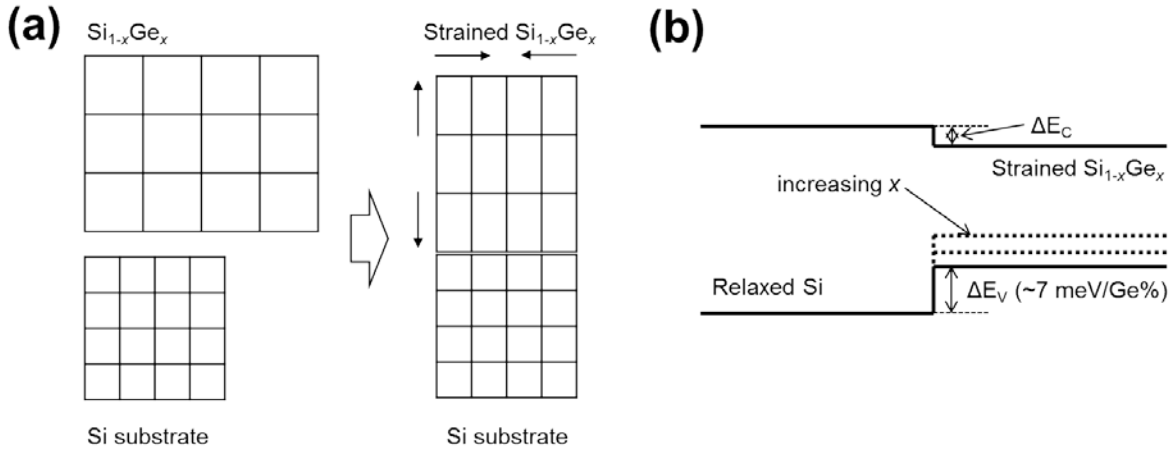

Figure 13 (a) schéma d'arrangement en treillis de l'tendues $Si_{1-x}Ge_x$ grandi dans le substrat Si. (b) un décalage de la bande de valence de l'ordre de ~7 meV/Ge%.

Afin d'induire une contrainte mécanique, Si et Ge sont généralement utilisés avec des compositions variées, et un désaccord de maille de l'ordre de ~4.2 %. Lorsqu'un film de $Si_{1-x}Ge_x$ ayant un paramètre de maille plus important que Si, est déposé sur un substrat de Si, ce film adopte le maillage du Si dans le plan de croissance et est alors sous une contrainte biaxiale compressive, comme illustré sur la Figure 7 (a). De plus, il y a un décalage de la

bande de valence de l'ordre de ~7 meV/Ge% comme illustré sur la Figure 7 (b), ce qui a pour effet d'améliorer la mobilité des trous.

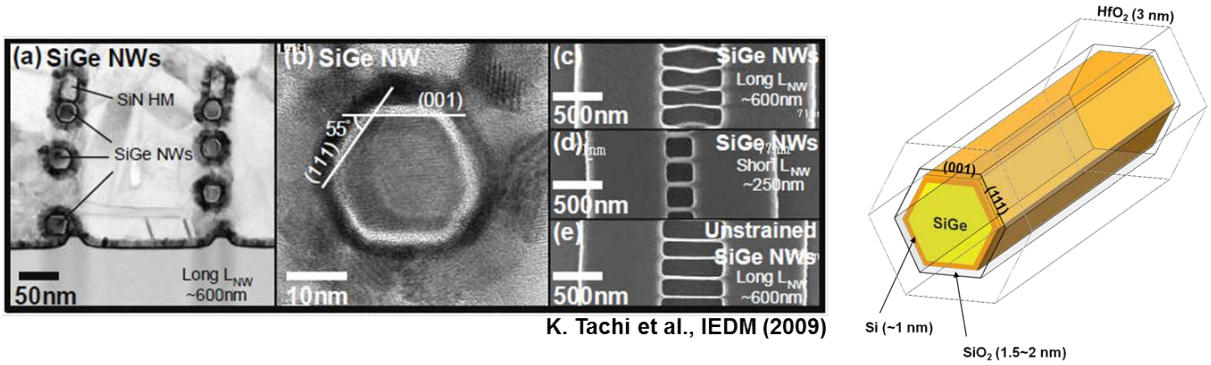

Figure 14 Images TEM et schématiques de la 3-D empilés compression tendues (c-tendues) Si / SiGe core-shell nanofils.

Pour des nanofils de SiGe, la forme est hexagonale, comme illustré sur la Figure 8, avec les côtés des facettes en {111}, vraisemblablement du fait du budget thermique nécessaire à la réalisation de la couche de Si d'encapsulation. On peut aussi noter la croissance d'une couche semblable à du $Si0_2$ de faible constante diélectrique d'interface (TIL: 1.5 ~ 2 nm) du fait que le procédé n'ait pas été optimisé. En ce qui concerne les dispositifs à canal long, ceux-ci sont courbés lorsqu'ils sont contraints (de manière compressive), alors que pour les canaux courts en SiGe, ils sont droits. Pour tous les dispositifs, le nombre total de nanofil est de 150 en parallèle (3 × 50 = 150). La largeur totale des dispositifs est ainsi estimée à environ 12.008 et 12.320 μm, pour les dispositifs contraints et non contraints, respectivement.

Sur la Figure 9, on peut remarque que la forme globale du bruit en courant normalisé varie en $(g_m/I_D)^2$ et pas en $(1/I_D)$. Ceci montre clairement que le bruit basse-fréquence dans les transistors à nanofils SiGe contraints ou non, peut être modélisé par un modèle de fluctuation de porteurs (CNF), et non par un modèle de fluctuation de mobilité (HMF). Il est intéressant de noter qeu pour ce qui concerne les transistors à nanofils SiGe non contraints, on a un bon ajustement avec le modèle de fluctuation de mobilité corrélée (CMF), alors que le modèle standard CNF suffit pour les dispositifs à nanofils SiGe contraints. De plus on constate que pour des courants de drain élevés, le bruit en courant normalisé décrois moins que $(g_m/I_D)^2$ du fait de la présence de fluctuation des mobilités corrélées additionnelles. Ceci signifie qu'il y a des effets différents qui influence le piégeage de charges dans le canal, suivant que les dispositifs sont contraints ou non.

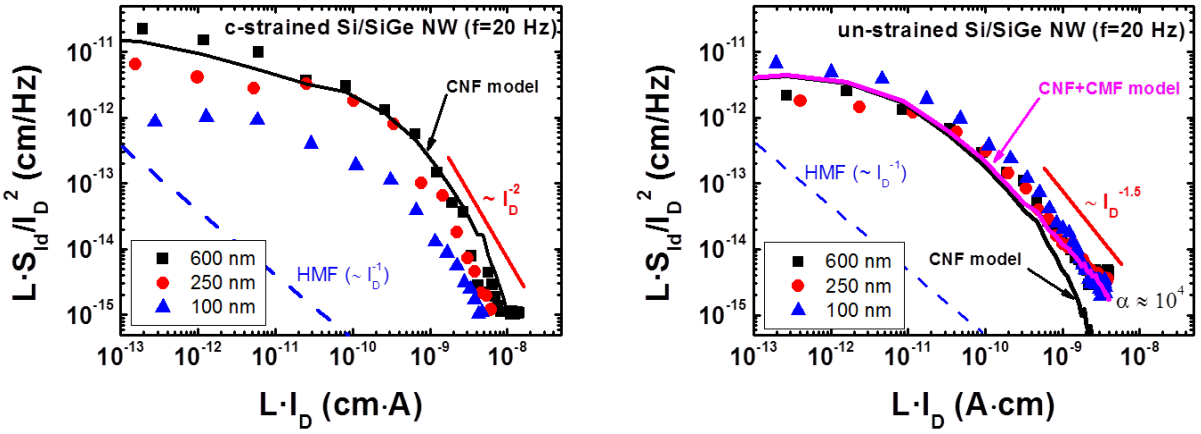

Figure 15 La forme globale du bruit en courant normalisé varie en $(g_m/I_D)^2$ et pas en $(1/I_D)$. les transistors à (a) nanofils SiGe contraints, (b) nanofils SiGe non contraints.

Pour confirmer l'influence des fluctuations corrélées de mobilité, nous avons extrait spécifiquement le coefficient de diffusion de Coulomb, α_C du modèle CNF+CMF en traçant la racine carrée du bruit de la tension de grille normalisé. Sur la Figure 10 (a), les valeurs extraites de α_C sont données en fonctin de la longueur de grille des composants. Pour ce qui concerne les nanofils SiGe non contraints, ce coefficient est légèrement supérieur à 4.10^4 Vs/C, tandis que pour les nanofils SiGe contraints, il est typiquement autour de 4.10^3 Vs/C, indiquant ainsi que les fluctuations de mobilités corrélées sont réduites de manière significative dans les nanofils contraints compressivement. Ceci pourrait sans doute provenir du fait que pour des canaux contraints il y a un meilleur confinement spatial des porteurs dans la structure SiGe cœur-coquille par rapport à une structure non contrainte. En effet pour une concentration de 20% de Ge on peut attendre un accroissement du décalage de la bande de valence de l'ordre de 100 meV. Les dispositifs non contraints ont donc un mode d'opération de surface plus important par rapport à ceux contraints compressivement, ce qui rend encore plus efficace la diffusion coulombienne, des charges à l'interface oxyde/couche d'encapsulation de Si, et ainsi accroît le coefficient α_C du mécanisme CMF. Selon la théorie de la diffusion coulombienne, une réduction d'une décade correspond à une distance supplémentaire de l'ordre de 1,7 nm pour les nanofils contraints, ce qui est en bon accord avec le fait que la couche de Si d'enrobage est de l'ordre de 1 ~ 1.5 nm.

Nous avons ensuite déduit la composante de la mobilité limitée par la rugosité de surface, μ_{SR} , à partir de la pente de la dérivée de l'inverse de la mobilité effective pour des tensions de grille importantes. Sur la Figure 10 (b), nous avons tracé les valeurs de μ_{SR} extraites en fonction de la longueur du canal pour une tension de grille de V_{GS} = -2 V. On peut constater

que pour les nanofils SiGe non contraints, μ_{SR} est trois fois plus petit par rapport aux nanofils contraints compressivement, ce qui reflète que la diffusion de rugosité d'interface est bien plus importante pour les dispositifs non contraints, ce qui est vraisemblablement dû au confinement accru des porteurs à l'interface oxyde/couche d'encapsulation de Si. Cela est cohérent par rapport à nos conclusions dressées à partir de notre analyse CNF+CMF du bruit, démontrant une atténuation du coefficient de diffusion coulombienne pour les nanofils contraints compressivement.

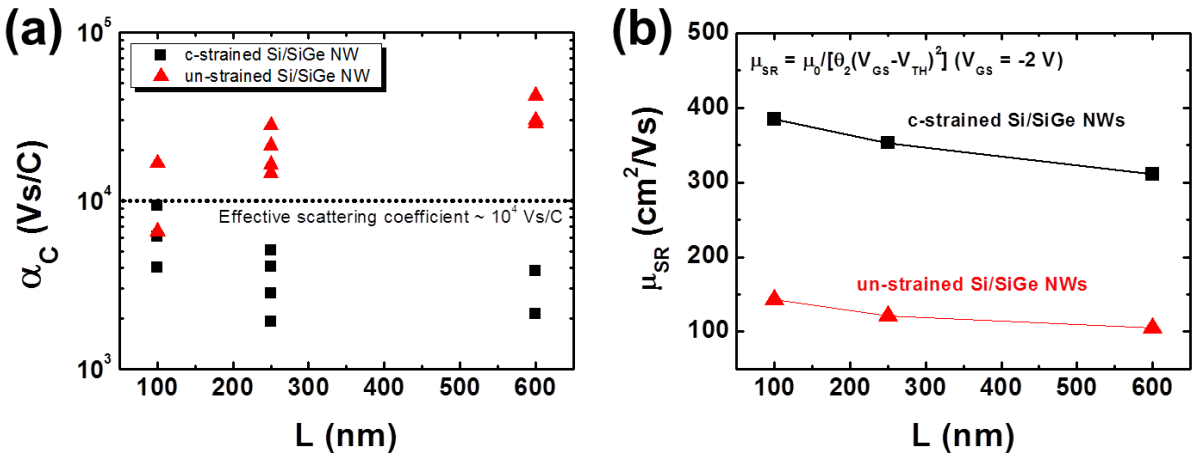

Figure 16 (a) les valeurs extraites de αC sont données en fonctin de la longueur de grille des composants. (b) les valeurs de μ_{SR} extraites en fonction de la longueur du canal pour une tension de grille de V_{GS} = -2 V.

En conclusion, le bruit basse-fréquence a été analysé et comparé pour des dispositifs p-MOS à base de nanofils SiGe cœur-coquille contraints et non-contraints. Nous avons trouvé que pour les deux types de dispositifs le bruit basse-fréquence peut être correctement interprété par le modèle CNF+CMF. Les nanofils SiGe non contraints ont un coefficient de diffusion coulombienne plus important, et une composante de mobilité limitée par la diffusion de surface plus faible. Ces caractéristiques cohérentes montrent clairement que les dispositifs à nanofils non contraints ont une mode d'opération avec une conduction plus en surface que ceux à nanofils non contraints, ce qui rend ces derniers plus sujets aux diffusions coulombiennes et de rugosité de surface. A l'inverse, les nanofils contraints compressivement bénéficient de l'architecture coeur-coquille, ce qui permet aux porteurs de charge de rester mieux confinés spatialement, plus loin de l'interface oxyde/couche d'encapsulation de Si.

B. Les jonctions métal-semiconducteur dans les dispositifs à nanotube de carbone multi-parois

Le bruit basse fréquence dans des nanofils de carbone multi-parois individuels (MWNTs) a été étudié pour différents types d'électrodes métalliques. Alors que le transport électronique dans les dispositifs à nanotubes se rapproche d'un transport quasi-balistique, le bruit devient prépondérant devant la résistance des dispositifs. Ceci montre qu'il y a une influence significative des contacts électriques sur le bruit électronique, suggérant dès lors qu'il est important d'établir un critère pour déterminer la qualité des contacts électriques dans les dispositifs à nanotubes.

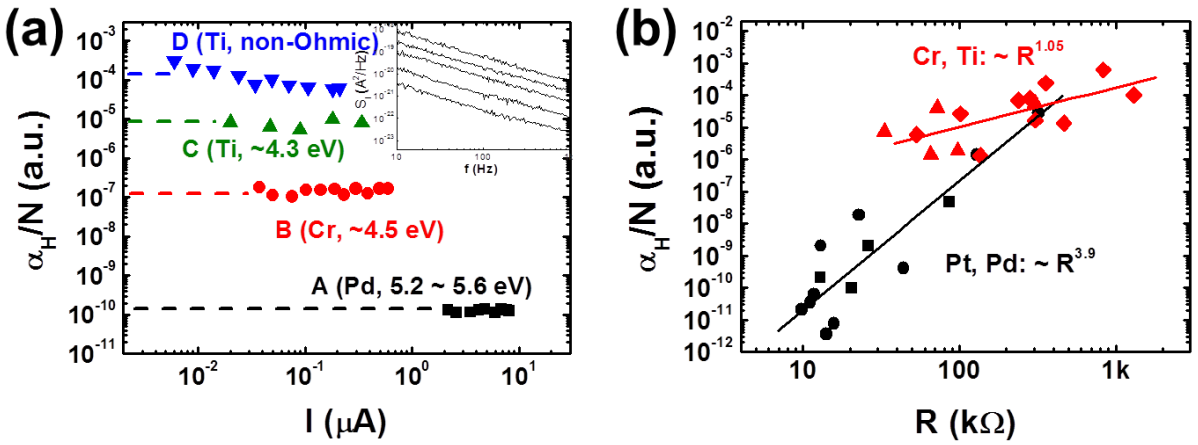

Figure 17 (a) l'amplitude du bruit α_H/N avec différents contacts métalliques. (b) l'amplitude de bruit en fonction de la résistance des MWNTs pour différentes électrodes métalliques.

Sur la Figure 11 (a), l'amplitude du bruit α_H/N a été utilisée pour comparer différents contacts métalliques car il était difficile d'estimer le nombre total de porteurs N dans les MWNTs. L'amplitude du bruit dans les contacts ohmiques est constant car il n'y a pas d'influence de la grille sur les dispositifs à MWNTs métalliques. Dans le cas de l'échantillon D, il y a une légère pente qui augmente avec le courant, ce qui peut être attribué à une dépendance différente du bruit en fonction du courant. Les dispositifs avec un contact en Pd qui ont une conduction quasi-balistique ont l'amplitude de bruit la plus faible, autour de 10^{-10}, alors que pour les contacts en Cr ou en Ti les amplitudes de bruit sont plus importantes, de l'ordre de 10^{-7} ou 10^{-5}, ce qui est en bon accord avec les résultats trouvés précédemment. En comparant les dispositifs à MWNTs avec contacts Pd et Cr, la différence de la résistance n'est simplement que doublée alors que le bruit pour les contacts Cr est 1000 fois plus grand par rapports aux dispositifs contactés avec du Pd, comme illustré sur la Figure 11 (a). Cette différence notable peut être visualisée sur la Figure 11 (b), qui montre l'amplitude de bruit en

fonction de la résistance des MWNTs pour différentes électrodes métalliques. Pour les composants avec des contacts Cr ou Ti, l'amplitude de bruit varie en fonction de $10^{-10,2}R^{1,05}$. Pour les contacts en Pd et Pt, le bruit chute rapidement avec la décroissance de la résistance, suivant une tendance en $10^{-26,3}R^{3,9}$. Du fait que les contacts électriques en Pd ou Pt montrent des caractéristiques de conduction quasi-balistique, l'influence des contacts sur le bruit devrait être plus restreinte par rapport au cas de contacts avec du Cr ou du Ti, ce qui indique une domination de la contribution du canal pour les contacts Pd ou Pt. Au final, nous confirmons que le bruit des dispositifs MWNTs à contacts en Pd et Pt reflète bien l'influence du canal de conduction avec un coefficient de forte resistance pour le spectre de puissance du bruit, différent pour des électrodes en Ti et Cr avec une contribution supplémentaire des potentiels de contact du fait d'un coefficient plus faible. Par ailleurs nous avons pu observer que le bruit est clairement en 1/ f quel que soit la nature des métaux ou le comportement ohmique des contacts.

IV. Bruit basse-fréquence dans les structures bi-dimensionnelles : transistor à effet de champ avec une monocouche de graphène

A. Structure et propriétés électriques d'un transistor à monocouche de graphène

Nous avons étudié des G-FETs, des transistors avec un canal en Graphène obtenu par CVD. Les composants ont été réalisé sur des substrats industriels de 6 pouces (150mm). Le substrat, dopé n^+ est recouvert d'une couche de 100 nm d'épaisseur de SiO_2 constituant la grille arrière. La graphène obtenu par CVD a été déposé par une technique de transfert. Les électrodes sont constituées de 100nm d'Au déposé sur le Graphène sans utiliser de résine photosensible afin d'éliminer l'influence des résidus de résine, mais avec une moindre qualité du contact électrique. Les différentes dimensions de longueur et de largeur de canal ont été obtenues en utilisant un procédé de gravure plasma. Les régions du canal ont été passivées par un dépôt de Al_2O_3 . La Figure 12 donne une vue schématique du dispositif ainsi qu'une photo d'un G-FETs.

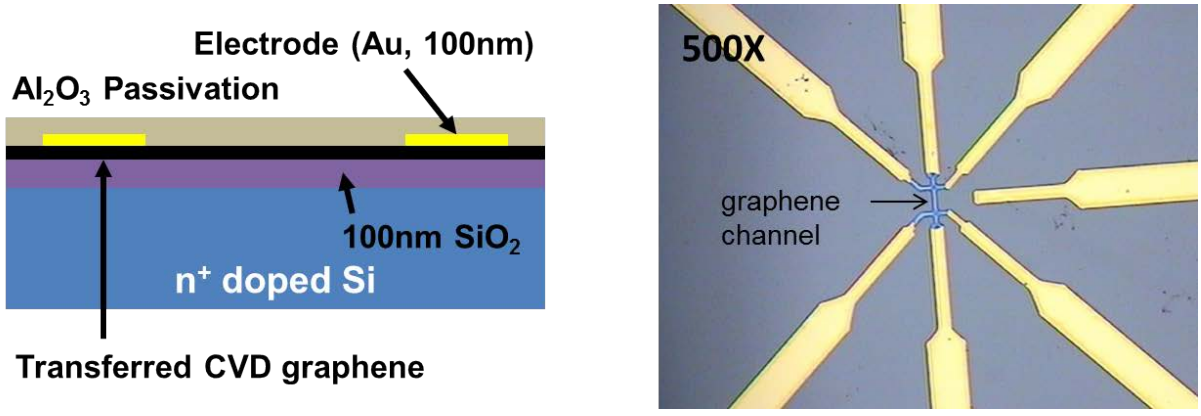

Figure 18 La vue schématique du dispositif ainsi qu'une photo d'un G-FETs.

Les propriétés classiques de transport électronique du G-FET ont été confirmées à travers des caractérisations I_D-V_{GS} et g_m-V_{GS} comme illustré sur la Figure 13. Nous avons déterminé g_m' ($=\partial g_m/\partial V_{GS}$) comme référence pour extraire la pente de la transconductance g_m pour des tensions de polarisation de grille importantes. A partir des courbes g_m-V_{GS} , la transconductance g_m augmente tout d'abord linéairement en commençant par le point de Dirac aux faibles tensions, puis comme à décroitre pour des tensions plus importantes (8 V et -12 V pour les électrons et les trous, respectivement). Nous avons pu estimer la concentration

de porteurs dans le graphène à partir de l'intégrale de la densité d'états qui augmente linéairement avec l'énergie à travers une distribution de Fermi-Dirac.

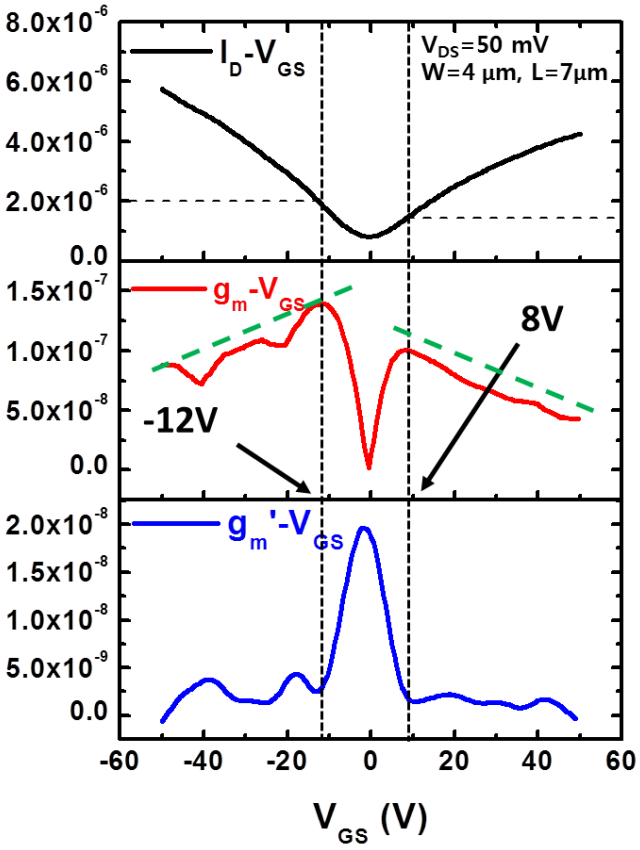

Figure 19 Les caractérisations I_D-V_{GS} et g_m-V_{GS} d'un G-FETs.

B. Bruit basse-fréquence d'un transistor à mono-couche de graphène

Nous avons mesuré le bruit basse-fréquence dans des G-FETs pour différentes tensions de grille. On observe un comportement général de type bruit en 1/f pour les différentes tensions de grille, mais il est sensible à la qualité des contacts. Ainsi si une pointe ne fait pas un bon contact lors de la mesure, on voit apparaître des caractéristiques de bruit originale. Sur la Figure 14, nous donnons la puissance spectrale de bruit en courant de drain pour les données brutes et les données lissées. Les inserts montrent les valeurs extraites γ et β définies par I_D^{β}/f^{γ}. Pour le paramètre γ, il est de l'ordre de 0.96, et le bruit S_{Id} augmente de manière proportionnelle à I_D^2 en fonction de la tension de drain, du fait que le courant de drain est linéaire avec la tension de drain.

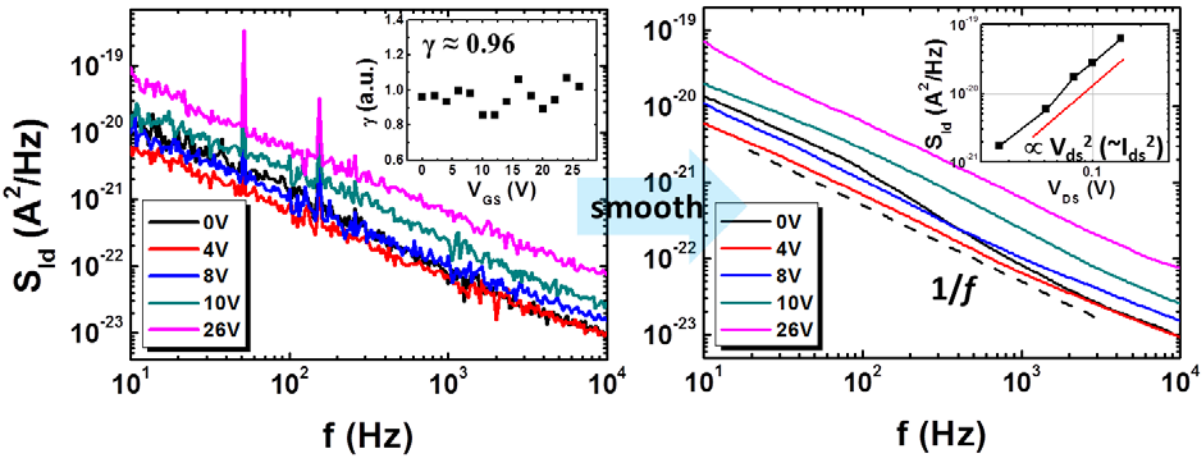

Figure 20 La puissance spectrale de bruit en courant de drain pour les données brutes et les données lissées.

Dans la région de type n du G-FET, le bruit en courant normalisé est comparé aux mod_les de fluctuation du nombre de porteurs de charges (CNF) et au modèle de Hooge de fluctuation de la mobilité des porteurs (HMF), comme illustré sur la Figure 15 (a). Nous avons ajusté le modèle CNF à partir de la relation $(g_m/I_D)^2$ des caractéristiques I_D-V_{GS} , mais il est en complet désaccord avec le comportement en bruit du Graphène. Ceci montre donc que le bruit ne provient pas du piégeage / dépiégeage des porteurs à l'interface Graphène/oxyde. D'un autre côté, de la même façon, le modèle HMF ne s'accorde pas correctement sur l'ensemble de la région étudiée, mais uniquement partiellement dans une région spécifique loin du point de Dirac. Sur la Figure 15 (b), la caractéristique du bruit est comparé au comportement de la transconductance g_m . Loin du point de Dirac, S_{Id}/I_D^2 suis une loi en $1/V_{GS}$ de manière identique à la région des fortes tensions de grille. Toutefois, près du point de Dirac, nous ne pouvons pas établir de corrélation claire avec la transconductance g_m .

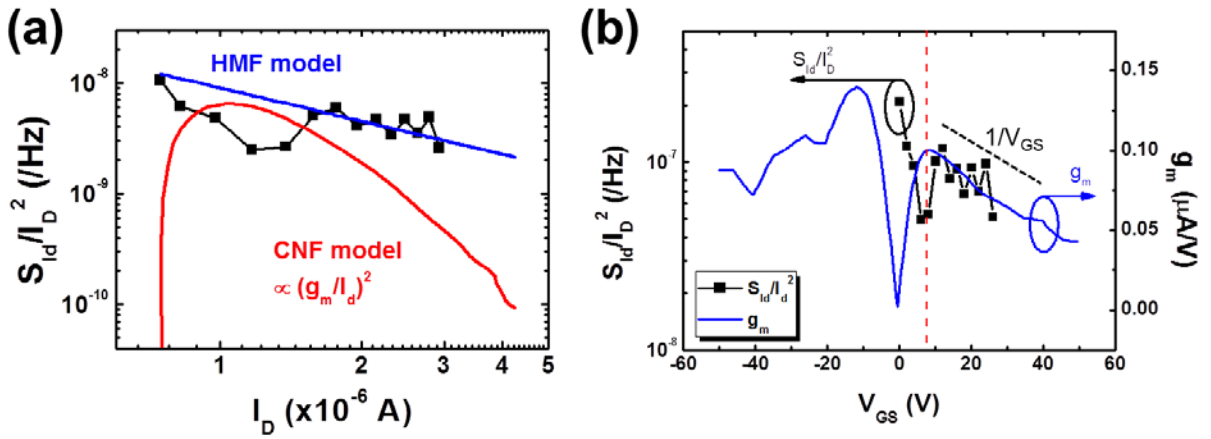

Figure 21 (a) le bruit en courant normalisé est comparé aux mod_les de fluctuation du nombre de porteurs de charges (CNF) et au modèle de Hooge de fluctuation de la mobilité des porteurs (HMF). (b) la caractéristique du bruit est comparé au comportement de la transconductance g_m.

Comme nous pouvons le voir sur la Figure 16, le comportement du bruit normalisé qui inclut les régions de type n et de type p, a la forme d'un 'M'. Cette caractéristique en 'Me est un comportement tout à fait original, caractéristique du bruit dans une mono-couche de Graphène. Le bruit en courant de drain S_{Id} augmente lorsque la tension de grille (et donc la concentration des porteurs) augmente, alors que le bruit en courant de drain normalisé S_{Id}/I_D^2 décroit. Loin du point de Dirac point, il semblerait que le bruit en 1/f noise dans le Graphène est fortement corrélé avec la mobilité de diffusion selon le nombre de couches. Ceci permet d'étayer l'ajustement partiel du modèle HMF. Toutefois près du point de Diract, nous pouvons supposer que l'origine du bruit est semblable pour des mono- et des multi- couches de Graphène, mais ceci reste à éclaircir. Nous envisageons l'effet d'une inhomogénéité spatiale près du point de Dirac.

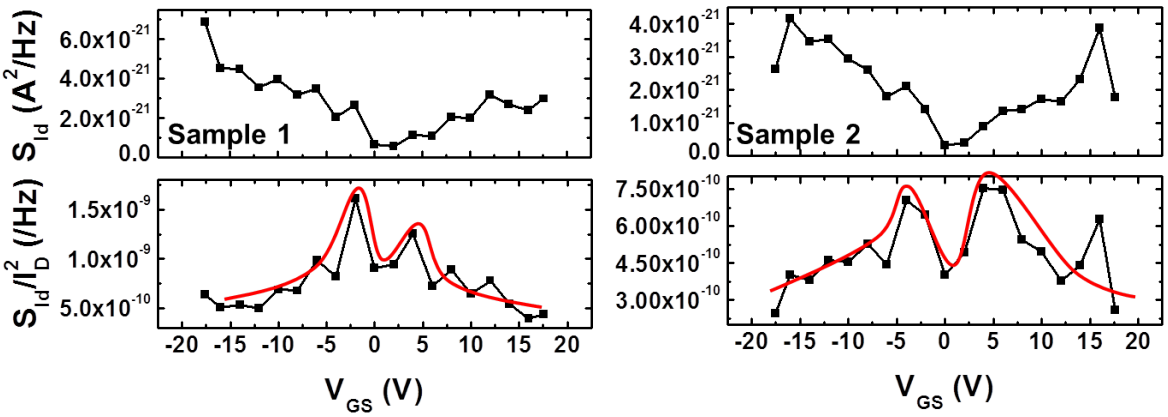

Figure 22 Le comportement du bruit normalisé qui inclut les régions de type n et de type p, a la forme d'un 'M'.

Nous avons aussi étudié des transistors FETs à mono-couche de Graphène obtenu par exfoliation mécanique par des mesures DC et des mesures de bruit basse-fréquence. Leurs propriétés électriques ont été analysées à partir du modèle électronique du transistor MOS. Ces transistors G-FETs exhibent trois types différents de transport selon la concentration de porteurs, et le bruit dans la région des faibles fréquence a un comportement de type 1/f. Nous avons essayé d'analyser le bruit à partir des modèles CNF et HMF, en variant la tension de grille, et nous avons pu montrer que les caractéristiques de bruit sont partiellement modélisables par le modèle HMF. Bien que cela ne soit pas très clair, le bruit basse-fréquence dans le Graphène pourrait être fortement corrélé avec le comportement de la mobilité.

V. Conclusion

Dans cette thèse, nous avons montré que les techniques de caractérisation en bruit basse-fréquence et en courant DC sont des outils puissants pour mieux comprendre la dynamique des porteurs de charge pour des structures de faible dimensionnalité. En réduisant la taille des dispositifs, alors que le courant de sortie décroit de manière assurée, le bruit lui ne décroit pas. Ainsi dans les dispositifs nanométriques, les études de bruit seront de plus en plus importantes pour comprendre les phénomènes et permettre de poursuivre la réduction d'échelle. Par ailleurs, certaines techniques de mesures (comme les mesures C-V) sont au niveau du point de rupture car trop imprécises ou inadaptées pour faire des mesures ou comprendre le comportement des dispositifs nanométriques. Le bruit basse-fréquence dans les structures de faible dimensionalité est fortement impacté par l'architecture du dispositif, les mécanismes de conduction, l'ingénierie de contrainte mécanique du canal, les jonctions métal-semiconducteur, et les structures de canal 2-D. La plupart des études de bruit ont été réalisé à température ambiante, mais des études à faible température bien que potentiellement intéressantes sont difficiles du fait de sources de bruits additionnelles, notamment liées au système de refroidissement. Bien que l'origine du bruit soit principalement dû au piégeage/dépiégeage des porteurs à l'interface ou dans le diélectrique, il ne faut pas pour autant négliger l'effet de la diffusion des porteurs. Ainsi des mesures de bruit à basse température seraient aussi intéressantes pour estimer l'influence de la diffusion des porteurs sur le bruit basse-fréquence.

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Patents

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1. D. Jang, J. W. Lee, G. T. Kim, L. Montes, and G. Ghibaudo, "*Electrical noise characterization in nano structure devices*", Workshop on III-V FET technology, Grenoble, France (2011.09).
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Dissertation for the Degree of Doctor of Philosophy

Transport properties and low-frequency noise in low-dimensional structures

Presented by

Doyoung JANG

School of Electrical Engineering

Graduate School

Korea University

December 2011

金 奎 兌 敎授指導

博 士 學 位 論 文

Transport properties and low-frequency noise in low-dimensional structures

이 論文을 工學博士 學位論文으로 提出함.

2011 年 **12** 月

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TITLE 1 - ADMINISTRATIVE TERMS AND CONDITIONS

1.1 Registration

Mr Doyoung, Jang (**date of birth: 28/Nov/1979) fulfils all the conditions required to register for a doctoral thesis in both institutions**....

Title of the degree allowing registration for a doctoral thesis:
or
Exemption from taking a Master's Degree: **12th november 2008 (EEATS committee)**

The administrative registration will take effect upon signing this agreement. It will be made each year in both institutions...

At INP Grenoble, registration will be made in micro-nanoelectronics*...* at EEATS doctiorate school

If necessary, complete with an equivalent sentence for the other institution.

1.2 Registration fees

The registration fees will only be paid in one of the countries; the institution that does not demand payment must have proof of payment in the other institution. For a given year, the fees must be paid to the institution where Mr Doyoung, Jang mainly resides time during the academic year in question, as detailed in the work periods defined in paragraph 2.1. At least one registration fee must be paid to one of the institutions.

- **In 2008/2009 academic year, the fees will be paid to the INP Grenoble**

- **In 2009/2010 academic year, the fees will be paid to Korea University**

- **In 2010/2011 academic year, the fees will be paid to Korea University**

.../...

1.3 Social security cover

Corresponding documentary evidence must be provided at the time of registration at INP Grenoble.

1.4 Accommodation and financial help provided to the student

One year grant for supporting stay in Grenoble will be given by Korea Univerity. IMEP-LAHC will also ask for specific regional grant (6 months) to complete the accomodation and grant support

TITLE 2 EDUCATIONAL TERMS AND CONDITIONS

2.1 Research work

Research work will concern: **Static and Low frequency noise characterization of one dimensional materials and devices**

Work will be supervised:

- **At INP Grenoble by Mr Laurent Montes , from the IMEP-INPG**

- **At Korea University, by Mr Gyu-Tae, Kim , from the Nano Device Lab.**

who agree to fully assume their supervising role for the doctoral student.

The work will be carried out:

Use the number of lines necessary. The time spent in each of the two institutions must not be less than a one year.

- **from 1/Feb/2009 to 31/Jul/2010 at INP Grenoble**
- **from 1/Aug/2010 to 30/Aug/2011 at Korea University**
- **from 1/Sep/2011 to 31/Dec/2011 at INP Grenoble**

2.2 Writing of the thesis

- **The thesis will be written in English**

Where the thesis is not written in French, a detailed summary must be provided in French.

- **A short summary, compulsory in France, will be written in both languages.**

2.3 Oral examination

The thesis shall lead to a single oral examination which will take place at INPG. ..The chief examiner of the jury shall draw up a record of thesis defence countersigned by the member of the jury.

This oral examination shall be recognized by both establishments.

Language of oral examination: the oral examination will include at least a short summary in French...

The thesis examining board shall comprise a well-balanced number of members from each institution appointed jointly by the contracting institutions and shall also include important persons not employed by these institutions. The examining board cannot have more than eight members.

..

- or an individually awarded doctorate from each institution:

- **INP Grenoble will issue the doctorate from the INP Grenoble, in accordance with French regulations,**
- **The Graduate School of Korea University will issue the diploma of Ph.D in accordance with Republic of Korea regulations……**

The statement in the doctoral certificate for the co-supervision program will follow according to the supplementary clause.

TITLE 3 – INTELLECTUAL PROPERTY

New knowledge shall be the property of the contracting party who obtained it, and will remain under its authority with respect to its use and publication.

TITLE 4 MODIFICATION - CANCELLATION

The present agreement can be modified or terminated by an amendment drawn up under mutual agreement and signed by the Principal and the Dean of each intitution……

Dated …

The Doctoral Student

Mr. Doyoung Jang

Supervisor at INP Grenoble

Dr. Laurent Montès

Supervisor at The College of Engineering at Korea University

Prof.. Gyu-Tae Kim

Principal of INP Grenoble

23/12/2008

Pour l'administrateur général
de l'Institut polytechnique de Grenoble
et par délégation
Le secrétaire général
Jean-François PICQ

Dean of The Graduate School of Korea University

Prof. Sung Shick Kim

TITRE

PROPRIÉTÉS DE TRANSPORT ET DE BRUIT À BASSE FRÉQUENCE DANS LES STRUCTURES À FAIBLE DIMENSIONNALITÉ

RÉSUMÉ

Les propriétés électriques et physiques de structures à faible dimensionalité ont été étudiées pour des applications dans des domaines divers comme l'électronique, les capteurs. La mesure du bruit bruit à basse fréquence est un outil très utile pour obtenir des informations relatives à la dynamique des porteurs, au piègeage des charges ou aux mécanismes de collision. Dans cette thèse, le transport électronique et le bruit basse fréquence mesurés dans des structures à faible dimensionnalité comme les dispositifs multi-grilles (FinFET, JLT…), les nanofils 3D en Si/SiGe, les nanotubes de carbone ou à base de graphène sont présentés. Pour les approches « top-down » et « bottom-up », l'impact du bruit est analysé en fonction de la dimensionalité, du type de conduction (volume vs surface), de la contrainte mécanique et de la présence de jonction metal-semiconducteur.

SPECIALITE

NANO ELECTRONIQUE NANO TECHNOLOGIES

MOTS-CELS

Transport électrique, bruit à basse fréquence, caractérisation électrique, extraction de paramètres, modélisation, simulation, transistors, nanofils, FinFET, transistor FET sans jonction, CNT, graphene

TITLE

TRANSPORT PROPERTIES AND LOW-FREQUENCY NOISE IN LOW-DIMENSIONAL STRUCTURES

ABSTRACT

Electrical and physical properties of low-dimensional structures have been studied for the various applications such as electronics, sensors, and etc. Low-frequency noise measurement is also a useful technique to give more information for the carrier dynamics correlated to the oxide traps, channel defects, and scattering. In this thesis, the electrical transport and low-frequency noise of low-dimensional structure devices such as multi-gate structures (e.g. FinFETs and Junctionless FETs), 3-D stacked Si/SiGe nanowire FETs, carbon nanotubes, and graphene are presented. From the view point of top-down and bottom-up approaches, the impacts of LF noise are investigated according to the dimensionality, conduction mechanism (surface or volume conduction), strain technique, and metal-semiconductor junctions.

KEYWORDS

Electrical transport, low-frequency noise, electrical characterization, parameter extraction, modeling, simulation, transistors, nanofils, FinFET, junctionless FET, CNT, graphene

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